DIGITAL OPTICALLY COUPLED TRANSIENT RECORDER

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CHAPTER 4

FIBRE OPTIC LINK

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DECLARATION

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ABSTRACT

This work is concerned with the investigation and development of a random-impulse acquisition system which combines a number of important features. These include fast acquisition, high speed digital transmission and recording. The design approach has been to divide the system into two sections; one operating in the harsh environment of the measurement point and the other in a relatively interference-free area. The two sections communicate through a high speed digital fibre optic link. The system is also designed to allow random 'single-shot' recording without the provision for an external trigger.

In the proposed system of this work, the high-speed digitisation of the signal being monitored is carried out at the point of measurement and the digital data is transmitted to the recording unit of the instrument via the digital fibre optic link. Such a system is far less susceptible to distortion than one which uses an analogue optical link where the digitisation of the signal is carried out at the receiving end of the link. The superior linearity provided by the proposed measurement system enables accurate traceable measurements to be achieved readily, whereas such measurements are difficult to accomplish with existing systems.

In this work a survey was made of the conductor-connected as well as optically coupled transient recording systems. The optically-coupled systems either used wide bandwidth analogue links or very low speed digital links. The suitability of a high speed digital system is studied. This involved a thorough investigation of the various parts of the system down to component level. The electronic circuits for the different sub-units of the digital fibre optic link were investigated using discrete components. Model parameter extraction for the transistors used was carried out using the s-parameter measurement technique. The results of this characterisation were used in the computer simulation programme, SPICE, to obtain reliable simulation results. The fibre optic link unit was implemented and tested successfully. The designs of the various sub-units of the high speed recording unit were investigated and the simulations of these were carried out using the digital simulation programme System-HILO. The simulation of the transient recorder unit circuits revealed that this unit would be capable of data recording at a rate of more than 100 Mega Samples/sec. Both simulation programmes used during this work for circuit analysis (SPICE and System HILO) were found to contain significant faults, the sources of which were identified and eliminated.

Subsequent testing of the complete system and the more detailed study of the recorder unit have shown that the system is capable of recording at the rate of 100 Mega Samples/sec. In these tests sinusoidal and chopped-impulse input signals were used. The chopped-impulse had a rise time of 1 μs and a chop time of 0.1 μs. The multi-wire technology of the circuit board of the recorder unit has been shown to be capable of high speed operation, but minor faults in the ADC driver and the RAM device have detracted from the completely successful operation of the system.

SYMBOLS AND ABBREVIATIONS

AC	Alternating Current
ADC	Analogue to Digital Converter
APD	Avalanche Photodiode
ASIC	Application Specific Integrated Circuits
BER	Bit Error Rate
c	Speed of light in free space
C	Stray Capacitance
CERL	Central Electricity Research Laboratory
CMOS	Complementary Metal-Oxide Semicondutor
CRO	Cathode Ray Oscilloscope
CRT	Cathode Ray Tube
DAC	Digital to Analogue Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DLE	Differential Linearity Error
DOCTR	Digital Optically Coupled Transient Recording
DSF	Dispersion Shifted Fibre
EB	Effective Bits
ECL	Emitter-Coupled Logic
ELED	Edge Emitting LED
EM	Electromagnetic
E_m	Maximum possible error
EMI	Electromagnetic Interference
FFT	Fast Fourier Transform
f_o	Bandwidth
FOL	Fibre Optic Link
f_s	Sampling Frequency
FSR	Full Scale Range
FWHP	Full width at half power
GHDL	Genrad Hardware Description Language
HP-IB	Hewlett Packard Interface Bus
HV	High Voltage
HZA	High impedance amplifier
ILE	Integral Linearity Error
LD	Laser Diode
LEAD	Linear Electronic Analogue to Digital converter
LED	Light Emitting Diode

LSB	Least Significant Bit
LV	Low Voltage
Mb/s	Mega Bits per second
m_r	Slope of ramp
MS/sec	Mega Samples per second
n	Number of bits of resolution of a converter
N	Number of converter levels
n	Refractive index
Nq	Quantization Noise
Nt	Total Noise
PC	Personal Computer
PD	Photodiode
PIN	Positive Intrinsic Negative
q	Quantizer step size
Q_n	Quantizer noise rms value
RAM	Random Access Memory
RF	Radio Frequency
rms	Root Mean Square
SINAD	Signal to Noise Ratio And Distortion
SLED	Surface Emitting LED
SNR	Signal to Noise Ratio
sr	Steradian
SUT	System Under Test
TDR	Time Domain Reflectometer
THD	Total Harmonic Distortion
t_s	Sampling Time
TZA	Trans-impedance amplifier
v	Speed of light in a dielectric media
VLSI	Very Large Scale Integrated circuits
WDL	Waveform Description Language

CHAPTER 1

INTRODUCTION

1.1 Introduction

Within any subject of study it is not until an adequate measurement technology has been put into place, that a thorough understanding of the subject becomes possible. In engineering, the need for traceable measurements is even greater in order to replicate devices and systems and ensure their reliable operation. The need for such measurements in systems which themselves create harsh electromagnetic environments is at last being recognised internationally. It is the purpose of this research programme to contribute to the ease of these measurements so that engineering and scientific progress can be encouraged not only by removing some of the tedious effort, but also enabling such characteristics of the measurand to be extracted which otherwise would have remained out of reach.

In this work a high voltage impulse acquisition system is proposed which is ideally suited for measurement in electrically hostile environments. The unique feature of the

proposed system is that it combined the high speed digital techniques and optical fibre communication to produce a system with which traceable measurement can be achieved readily. The objective of this work is to investigate the feasibility of such a system for HV impulse measurement under strong EM conditions.

In this chapter, the problems associated with measurement in electrically hostile environments are outlined. The advantages of the optically-coupled systems in avoiding such problems are then presented briefly. This is followed by a discussion of optically coupled systems using analogue links and their drawbacks. Systems using digital links, however, do not suffer from the difficulties associated with analogue links. The investigation of such digital systems is the subject of this work and the proposed Digital Optically Coupled Transient Recording (DOCTR) system is then briefly introduced. The merits of this system and the need for this work are also discussed. A brief outline of the investigation of this work as well as the objectives and plan of the thesis are then presented.

1.2 Measurement in Hostile Environments

The traditional approach for measurements of electrical signals in hostile electromagnetic environments is to use high signal levels to ensure an adequate signal-to-noise ratio (SNR). This is illustrated, for example, in high voltage oscillographic measurements where surge measurement CROs may have input signal voltages of several kV. Until the advent of digital techniques in modern electronic equipment, such as analogue-to-digital converters (ADC), there seemed little need to change this. The only pressure for change was that such measurements were increasingly unable to justify, economically, the manufacture of such instruments. This latter problem was exacerbated by the fact that such measurements were invariably random "single-shot" ones necessitating high writing speeds.

The use of solid-state based devices, which have input voltage ranges of a few volts, in environments such as a high voltage laboratory requires extensive screening to produce

an acceptable SNR with respect to the lower input signal levels. The reduction of the "noise" signals is a very difficult and crucial problem; elaborate preventive measures are needed to ensure the required accuracy of measurement [Thornton,1991; Malewski and Poulin, 1985; Martin,1979]. The difficulties are compounded in high voltage (HV) impulse measurements. Steep-fronted impulses are accompanied by strong electromagnetic (EM) fields which have a rapid rate of change. Measurement systems must have adequate protection against rapidly changing fields. Long lengths of coaxial cables used in measurement arrangements are particularly susceptible to such fields.

In addition to noise reduction, ground loop currents cause voltage variations in the reference plane, resulting in measurement error, and this is another aspect which has to be dealt with by careful circuit arrangement. The solutions require great experience and usually demand expensive screening. Some of these problems are inherent in the system e.g. large connected earth systems must have disturbance waves travelling within them. Although much can be done by careful single point earthing, a conductor-connected oscilloscope or recorder is vulnerable to these 'earth conductor' potential changes if these common mode signals can reach its sensitive parts. Thus even a potential-divided input does not reduce this ground potential variation sensitivity.

1.3 Existing Optically Coupled Measuring Systems

An attractive way of overcoming these difficulties is to use a fibre optic link (FOL) to 'isolate' the oscilloscope or recorder from the measurement point. This not only overcomes any difficulty due to EM coupling with data carrying cables, but it also eliminates the problem of common paths and associated heavy currents. The question which remains when using a FOL-based system, is the integrity and reliability of the FOL for the measurement.

A relatively simple FOL-based system is that using an analogue FOL. In this case the signal is transmitted through the FOL in analogue form and the digitisation of the signal is carried out at the receiving end of the FOL using a digital scope [Miller et al,

1987, Halkiadis et al, 1991] or a purpose built digitiser/recorder unit [EOD,1988; Van der Sluis, 1989; Nicolet,1991]. With such a system the integrity of the signal being monitored is dependent on the linearity of the analogue FOL and as the FOL has a relatively poor linearity, the accuracy of the measurement is therefore limited. The performance of an analogue FOL is also dependent on the linearity characteristics of the optical source. In such cases the FOL must be calibrated before a measurement can be carried out [Miller et al, 1987]. Even then the analogue FOL could be the 'weakest' part of the measurement system [Van der Sluis, 1989]. Any minor physical strains on the fibre may also effect the characteristic of the fibre which directly affects the linearity of the analogue FOL. These non-linear effects mean that system response corrections cannot be relied upon when an analogue link is used. Such problems are faced in practice when using, reputable, analogue-FOL-based systems in industry [Noe,1993; Holden,1993].

The reported measurement systems using digital links fall into two categories depending on their characteristics. One type [Dyer and Holbrook, 1986] is reported to be capable of high digitisation rate, but required a repetitive input signal. The other [Murphy,1990] was capable of transient capture but with a maximum rate of 5 MS/sec. None of these digital systems could be suitable for HV impulse measurement.

Two conditions are required to be met for digital HV impulse measurements: the digitisation rate to be high enough to capture HV impulses with given accuracy [ANSI/IEEE-1122, 1987] and the ability to produce traceable measurements. This work investigates the feasibility of a digital optically coupled system which combines these two features.

1.4 The DOCTR System

The difficulties mentioned above and the requirements needed for accurate and reliable measurements initiated the idea of the work presented here [Olyabek and House, 1991]. In this work a recording system is proposed which uses a high speed digital

FOL as the link between the two separate parts of the system. The block diagram of the proposed Digital Optically Coupled Transient Recording (DOCTR) system is shown in Fig 1.1. The design approach has been to divide the system into two parts; the digitising signal capture unit (hereafter referred to as the capture unit) and the receiver/recorder unit (hereafter referred to as the recorder unit). The two sections of the system communicate through the digital FOL. The digital FOL provides a linear channel of communication and the integrity of the data is unaffected by the transmission through the digital FOL. With such a system the digitisation of the signal being monitored is accomplished at 'source', the point of measurement, and the digital data is transmitted via the digital FOL. At the recorder end the incoming data is stored in high speed RAM devices. This is in contrast to many other systems [Miller et al, 1987; EOD, 1988; Van der Sluis, 1989; Nicolet, 1991] where an analogue link is used to transmit the signal to the recorder unit and then the signal is digitised.

The digital FOL is less prone to the effects of physical strains on the fibre cable and more importantly, it does not suffer from the non-linearity effects in the analogue transmission. The capture unit may be operated in the vicinity of the system under test (SUT), as it is adequately screened to protect the sensitive electronic devices. The recorder unit can operate in a relatively interference-free zone and no special shielding precautions are necessary.

1.5 Merits and Attributes of the DOCTR System

Measurements at extremely high potential difference is possible with such a system because of the electrical isolation provided by the FOL. In addition, the data being transmitted through the fibre is immune to EM interference, since the fibre cable is not subjected to EM coupling. Measurement problems due to ground current loops which lead to high voltage coupling on cables, resulting in the introduction of 'noise' in the system are simply not present with FOL-based systems.

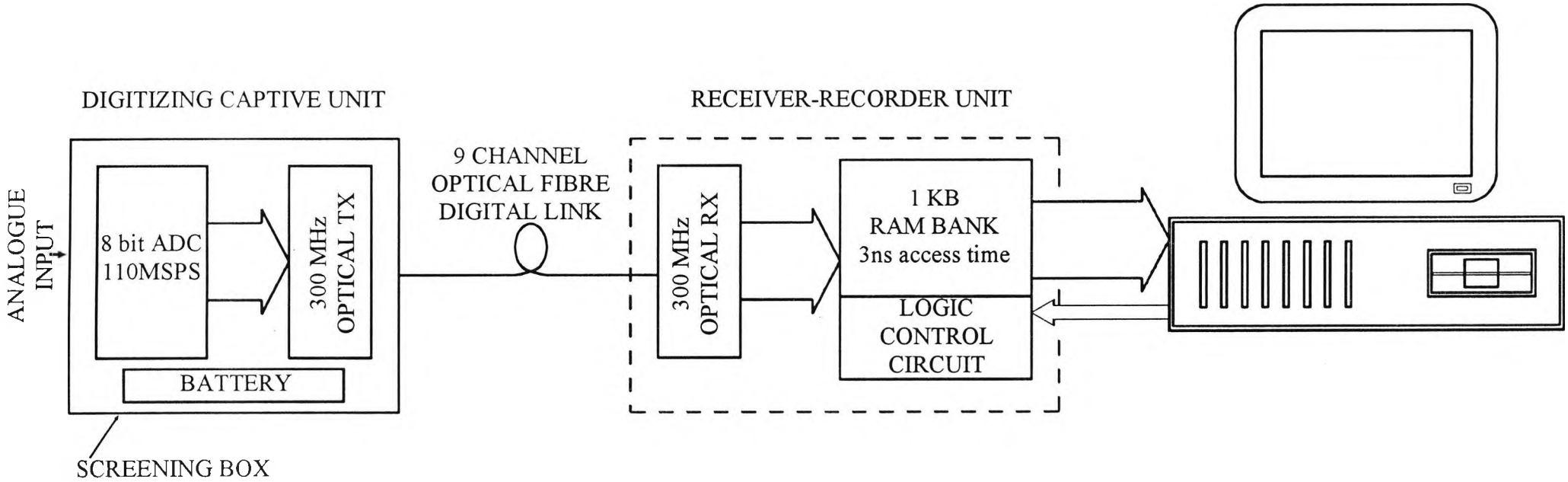


Fig 1.1 Block diagram of DOCTR

The use of the digital FOL means the system does not suffer from the non-linearity effects of an analogue link. In this system, the digital FOL as well as the remainder of the system, i.e. the recorder unit, has a linear characteristics and the only unit of the system which has to be calibrated is the digitiser in the capture unit. In view of the importance of traceable measurement, all that is needed in the DOCTR system is a measure of the traceable measurement of the digitiser only .

The ease and reliability with which such (traceable) measurements can be carried out is a significant aspect of the DOCTR system in evaluating the characteristics of HV circuits (e.g. an HV divider). With such a system, any response correction needed may be achieved reliably. For a linear system such as this, separate responses can be summed to get the total response as used in FFT techniques. This is not possible with a non-linear system.

The optically coupled systems reported or those commercially available either have wide bandwidth analogue links (of several 100 MHz) or low speed digital links (a few MHz), which is not adequate for fast HV impulse measurement. The digital FOL of the DOCTR system is capable of more than 300 Mega Samples per second (MS/sec).

The recorder unit of the DOCTR system facilitates random transient recording, enabling 'single shot' measurements without the provision of external triggering. It also allows a programmable view of the 'pre-event' history of the signal.

As an alternative to bulky and conventional instruments, the small size of the capture unit allows access to remote or hard-to-reach locations where it would be impossible to use conventional recorders or oscilloscopes. The capture unit is small enough not to seriously perturb the SUT and, since it has its own battery supply, it may be treated as part of the SUT.

1.6 Scope and Objectives of the Thesis

In response to the difficulties faced in measurement in hostile electrical conditions, this work was under taken to investigate a measurement system with which some of these difficulties are avoided. This thesis presents results of studies carried out to produce a desirable piece of measuring equipment which removes the need for a very expensive, sophisticated and specialised measurement environment as well as equally skilled staff to operate it .

The task of developing such a system and the problems associated with the design and implementation of high speed circuits cannot be underestimated. The minimum speed of operation had to be maintained throughout the system at the rate of 100 MS/sec; from the digitiser, through the optical link to the storing of data in the recorder unit. The difficulties were compounded by working at "developing" technologies and the difficulties in obtaining the devices required and reliable supplies for those devices. Introductory samples of recently developed state-of-the-art products had to be investigated during this work to test their suitability for incorporating them into the system. On a number of occasions the investigation and design work on such products had to be abandoned because of the manufacturers ceasing to produce them. On one occasion, after the construction and testing of a complete unit, it had to be set a side because the required components had become obsolete. This naturally makes the construction and testing of the whole system extremely difficult. However different parts could be simulated and tested.

There are different design constraints for high speed circuits compared to similar circuits operating at low frequencies. Many features of circuit components which are not normally significant and therefore are not considered in the design of low speed circuits, play a crucial role in the high frequency circuits. Propagation delays and rise and fall times of even the fastest devices become significant for high-speed operation of a circuit and such characteristics and their variations have to be allowed for during the design stages of the circuit.

The high speed operation of circuits may be inhibited by the packaging of the devices used in them. Small-outline packages are therefore used to lessen the stray capacitive and inductive effects of the package. For still higher frequencies, the device die is used directly in the circuit to reduce these effects still further.

The DOCTR system operates at high speed and hence signals propagating through signal tracks on the circuit board are subject to crosstalk or mutual interference between the individual tracks. These effects are especially severe the more rapid the switching of the signals. This consideration required particular attention when designing the DOCTR system.

The development of any high speed measurement system involves the design, simulation, construction, testing and evaluation of the various units of the system. The design and simulation of the units of the DOCTR system are particularly important because of the speed of operation of these units. The simulation of the high speed circuits is essential in identifying the limitation of such circuits. The simulation process leads to the requirement of detailed analysis of the characterisation and modelling of the components used in the various circuits. Correct simulation results are only obtained if accurate component models are used. This work essentially covers the design and simulation of the digital units of the DOCTR system although construction and testing of some of the units have also been accomplished. Various designs have been suggested for the circuits of the FOL and recorder units and those most suitable for this application considered in detail. The transmitter and receiver circuits in the FOL unit were designed, simulated and constructed using discrete surface mount components. A later version of the FOL unit was constructed using hybrid integrated circuits. The digital circuits of the RAM and control circuits of the recorder unit were designed and simulated and used integrated circuits (IC's). The construction stage of the recorder unit required an investigation into the fabrication of circuits boards capable of operating at high speeds. This is to evaluate the level of crosstalk between adjacent signal tracks.

This work involved investigations at component and circuit level as well as at system level, but the large amount of the detailed work does not allow its inclusion in the limited space of this thesis. Detailed analysis such as those of the transistor circuit designs of optical transmitters and receivers, using hybrid-π model are not presented here, but only the outline of the work done and the results and conclusions obtained.

The recorder unit is to be interrogated by the computer and be re-armed after the data has been retrieved from it. The user must also be able to select the preset conditions of the recorder unit. This is achieved through a software program developed specifically for these functions.

The objectives of the work are to:

- Determine the digitiser characteristics required for HV impulse measurement.
- Investigate the design, simulation and construction of a FOL unit required for this system.
- Investigate the design, simulation and construction of a recorder unit and the associated circuit to facilitate the features required for this system.
- Develop the software needed to program the operation of the recorder unit as required.
- Incorporate existing up-to-date commercial sub-units in the system so that it could readily go to production.
- To test the DOCTR system and evaluate its performance.

1.7 Structure of the Thesis

From the functional point of view the DOCTR system consists of three units; the digitiser, the FOL and the recorder unit. Each of these units is described in a separate chapter and the design, simulation and construction of each is discussed at the end of corresponding chapter.

Chapter 2 covers the discussion on the measurement difficulties encountered in noisy EM environments such as the HV laboratory and the measures taken to reduce the effect of sources of error. A survey is then presented in this chapter of the conventional systems used for impulse measurement in such environments and the measurement difficulties associated with them. Light-based systems are then reviewed which are used for general measurements in harsh environments. The review of optically coupled systems are grouped in the two categories of analogue and digital systems. An overview of the DOCTR system is given towards the end of this chapter.

Chapter 3 presents a review of the different types of digitisers and discusses the characteristics required for HV impulse measurement as well as the sources of errors in those applicable to HV impulse measurement applications.

Chapter 4 covers the discussion on the fibre-optic-link. It presents the discussion on the characteristics of the different types of optical fibre as well as those of the optical source and detector. A review of the various optical transmitter and the receiver circuit designs is presented. It also presents the analysis and design of the transmitter and receiver circuits and their corresponding simulation results. The noise analysis treatment of the optical receiver is emphasised because of its importance to the performance of the receiver. The construction and test procedures of the circuits involved in the FOL are outlined towards the end of this chapter.

Chapter 5 covers the investigations into the development of the recorder unit. It outlines the circuit designs for the different RAM organisations which were to be used at different stages of the work and presents the final design in more detail. The speed

of operation of the recorder unit and the critical nature of the timing criteria at such speeds requires careful component layout arrangements and suitable choice of board technology for the recorder unit circuit board. These requirements are also covered in this chapter. The programming of the digital simulation package (System HILO4) is discussed and the simulation of the circuit design is given towards the end of the chapter.

In Chapter 6 the construction details of the capture unit and the design details of the shield or the screening box are presented. The predicted screening properties of the shield is also given. The arrangement of the digitiser, the transmitter end of the FOL, the batteries and the control and regulating circuits and their corresponding designs are presented in this chapter. The construction of the recorder unit and its associated control circuit are also given in this chapter. Also included is a discussion on the interface circuit between the recorder unit and the PC which interrogates the former when the correct data is recorded. The software developed to program the recorder unit through the PC is also presented in this chapter.

In chapter 7 the results of tests on the individual units of the DOCTR system and also those for the complete system are presented and discussed.

Finally, the conclusions and the recommendations for further work are given in chapter 8.

CHAPTER 2

SYSTEMS OF MEASUREMENT IN HOSTILE E.M. ENVIRONMENTS

2.1 Introduction

Electrical measurements in hostile EM environments such as an HV laboratory are affected by interference problems. Because of the high levels of the voltage or current involved, they can become the source of gross interference and noise levels which may seriously affect the monitoring system and therefore the measurement accuracy. The problems are compounded for impulse measurement because of the fast rates of change. These have resulted in a particular awareness in the community of HV/Power engineers and researchers about sources of error in HV impulse measurement and the measures required to prevent or reduce the effect of those sources. The steps taken to reduce the effects of these noise sources are now well established [Hylten-Cavallius

1969; Morrison, 1977; Martin 1979; Hylten-Cavallius 1984; Thornton 1991] but are quite expensive to implement. Studies have been carried out to evaluate the level of interference prevailing in such environments in order to take these into account in the design and shielding of electronic instruments and also in the physical arrangements of test equipment [Malewski et al 1982; Russell et al, 1984:a; Russell et al, 1984:b]

Relatively recent advances in fibre optic communication have had a direct impact on measurements in electrically harsh environments and have led to important advances in the design of instrumentation for such applications.

In this chapter typical sources of errors in measurements in hostile environments such as HV laboratories and substations are first considered and then the preventive measures taken to reduce the effects of those sources of error are outlined. This is followed by a review of the conventional systems used for HV impulse measurement and monitoring of surges in power systems. A brief discussion of the grounding and shielding techniques employed to reduce various sources of interference and to ensure the correct operation of these systems is also presented.

Before considering the optically coupled transient recording systems, general 'light'-based systems used in HV/Power substation environments are reviewed with emphasis on fibre optic applications in HV and power system instrumentation. A review is then made of optically coupled transient recorders which are designed for measurement in noisy environments. These recorders are considered separately depending on the type of the FOL used; analogue or digital.

Finally, an overview of the DOCTR system suggested in this work is also presented.

2.2 Sources of Measurement Errors in HV Environments

The sources of errors in impulse measurement in electrically hostile environments are due to interferences caused by the electromagnetic coupling and common ground circuits or 'loops'. The EM coupling may be considered in terms of radiative coupling

for rapidly changing voltages or in terms of quasi-static capacitance and magnetic field coupling between electrical cables linking the monitoring system to that under test, for slower signals. Such conductors are one of the prevailing sources of difficulties in that they pickup unwanted interference by both electrostatic and magnetic means and convey such interference directly into the electronic measurement system.

Apart from inductive and capacitive modes of coupling, another form of coupling is associated with the conductor links. This can play a dominant role in the interference and is brought about by the impedance of common conductors. Such links may form part of a ground loop through which heavy currents, of the order of several thousand amperes, flow and these can introduce voltages of the same magnitude as the signal being transmitted through, say, the core of the cable.

Ground loops are formed by multi-point ground connections in a circuit. Through a ground loop, unwanted voltage signals commonly known as noise, will enter the system causing measurement error or false triggering etc. The potential difference in the loop drives a substantial current through the inductive impedance of the loop which in turn may induce a significant voltage into the monitoring system.

Consider a typical HV circuit such as an impulse generator and its associated supply and monitoring system units (Fig 2.1). A power supply unit is required to charge the capacitors (not shown) and to supply the trigger and control units. These will have ground returns. The trigger unit link to the spark gap uses a coaxial cable with its braid grounded. The coaxial cabling linking the low voltage (LV) section of the potential divider to the CRO will also have its braid connected to earth. The mains supply to the CRO will also have leads connected to ground.

A ground loop is formed by the braid of the coaxial cable through the CRO body to the mains ground and from these to the case of the trigger unit continuing through the braid of its coaxial cable back to the circuit. Potential difference of the order of several kV may exist between the various ground connections even though they are attached

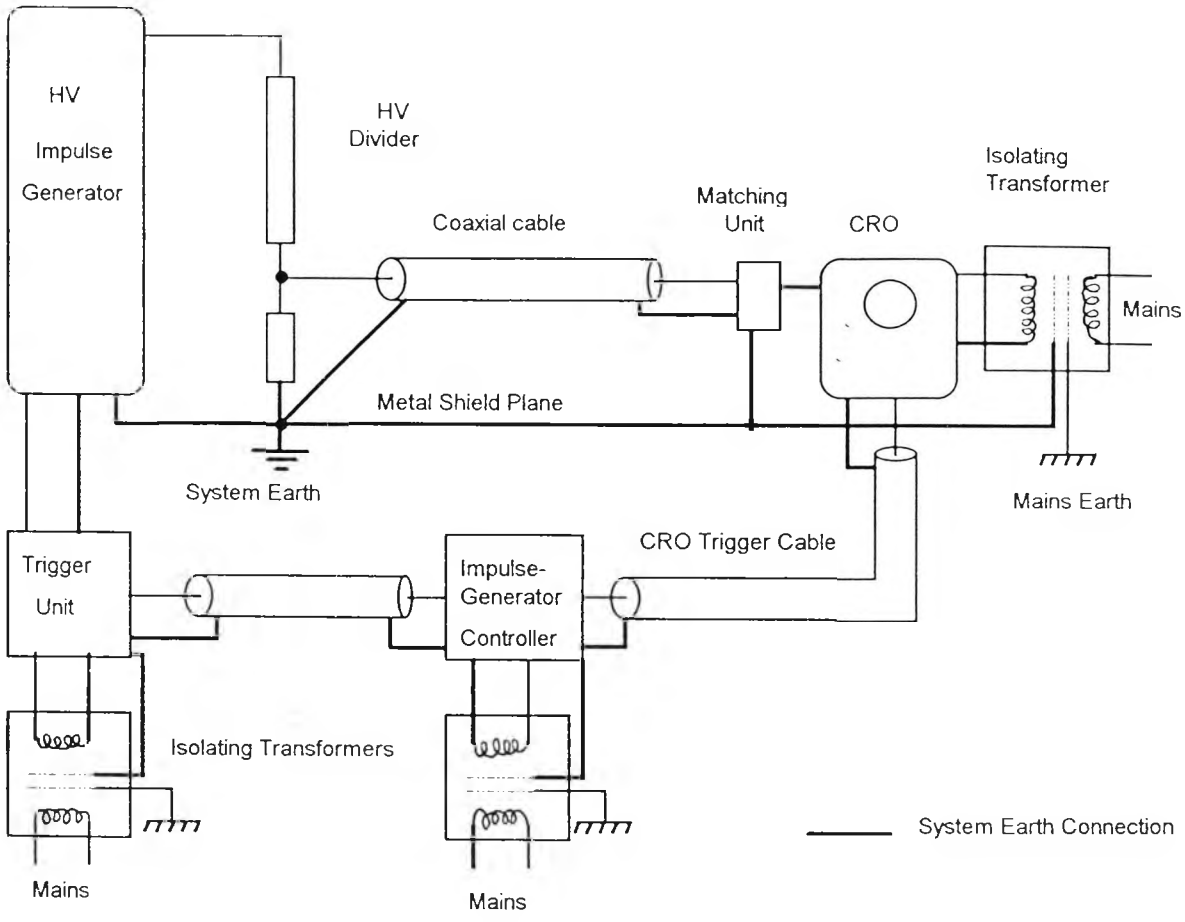


Figure 2.1 HV circuit showing monitoring systems and supplies

only 10 cm apart on a 10 cm wide connector [Thornton,1991]. This could lead to a loop current of several hundred Amperes depending on the (inductive) impedance of the particular loop. In practice the loop path, including the total coaxial cable length, may be several meters long having a loop impedance of several ohms.

Such surge currents in the housing of the CRO or a monitoring system could result in a change of potential difference in the system's reference plane. Elements at earth potential during steady operation can temporarily acquire a high potential which can cause damage to the equipment. This kind of interference could undermine the operation of the monitoring system and results in errors the recorded data.

In addition, in the case of the coaxial cable linked to the CRO, since the braid is imperfect, the braid current induces a signal into the coaxial cable conductor and therefore affects the data being transmitted through the cable. Such interference could affect digital as well as analogue connections to modern electronic instrumentation which operate with relatively low input signal levels. Traditional HV impulse monitoring equipment had input signal levels of the order of 1 kV so that they would be less susceptible to such interference.

Digital links can offer superior signal-to-noise ratio (SNR) performance to analogue ones, in the sense that the former are insensitive to low levels of interference or noise since only two binary levels are transmitted through the link compared to the continuum signal levels which have to be transmitted through the analogue link. However when relatively high levels of interference are introduced, i.e. of the order of, or higher than, the voltage swing between the two binary levels of the digital system, then digital links do become susceptible to such interference. The voltage swing between the two binary levels (High and Low) of a digital system based on ECL logic technology is 0.8V. For a coaxial cable with a transfer impedance of 10 mΩ /m and a length of 5 meters, a braid current of 100A will induce a voltage level of 5V onto the core of the cable. Under such conditions the data will be subject to corruption while being transmitted through such a coaxial cable. Even when using a screened cable it is

important to ensure that additional ground loops are not created unintentionally. In this case, the braid is in effect acting as a shield and a source of interference at the same time. Controlling the ground loops is therefore of paramount importance in order to reduce interference in the circuit. In practice it is often difficult to identify and control these. Ground loops may comprise not only the main circuit leads and diagnostic cables, but also involve the whole of the mains wiring of the surrounding building.

Stray capacitance may also play a crucial role in admitting interference into the circuit. A stray capacitance may exist between the output of an impulse generator and the surrounding (wall, ground), with a typical value of 10 pF. A 500 kV impulse rising in 100 ns will result in a current flowing through the 10 pF stray capacitance of:

$$C\frac{dV}{dt} = 10^{-11} \times \frac{5 \times 10^{5}}{10^{-7}} = 50A$$

For a low ground loop impedance (less than 1 μH) a current will flow through the loop resulting in interference as discussed earlier. For a high ground impedance (more than 10 μH) the ground potential will rise by tens of kV during the impulse duration. This will in turn result in interference in the circuit.

In some reported discharge measurements [Hampton, 1988] conductor linked systems would be almost impossible to use because of the affect of large reference plane voltage variations on the operational performance of the measurement system.

2.3 Preventive Measures to Reduce Sources of Errors

Careful and vigorous steps must be taken and sometimes elaborate and expensive arrangements are used to ensure that the effects of such interference is minimal. Some of the measures taken to reduce the effects of ground loops are as follows:

- Multiple point grounding must be avoided. This is important to be applied within the low voltage side of the system as well as the HV side. Multiple grounding at the instrumentation or signal monitoring section of the system could also lead to the

disturbance of the measurement in addition to creating global ground loops in the system.

- The ground current loops may sometimes be interrupted by the use of inductors, thus raising the impedance of the loop path. Provided that the high impedance introduced into the ground loop does not impede the normal function, this is a particularly simple and useful technique. e.g. in power supply leads which are not carrying high powers. In the case of coaxial cables the sheath inductance can be considerably increased by coiling the cable round a large ferrite toroid, without affecting the character of the cable itself.

- Floor metal sheets or nets are used as ground return in HV test areas, and to screen signal cables connecting impulse generators to monitoring/recording systems.

- Isolating transformers are used in the power supplies. Interference difficulties are not entirely avoided because of the capacitance between the screens of the primary and the secondary windings which results in coupling between the mains earth and the 'isolated' supply as shown in Figure 2.2 [Morrison, 1977].

A careful and thorough inspection and analysis of the circuit and system layout is required with the aim of eliminating or reducing the ground loops. This must be carried out while ensuring that the steps being taken do not, under any circumstances, conflict with safety or with the provision of an overall ground connection to the system which provides low impedance path at DC and mains frequency. Engineers with extensive experience in this field have a vigorous and step-by-step approach to reduce the effects of such sources of interference [Martin, 1979; Thornton,1991]

To prevent conducted interference through leads, all cables must be screened preferably using solid metal and must be as short as possible since long cables are more vulnerable to EM coupling. Cable connections to instruments must maintain completely continuous screening from the cable to the instrument.

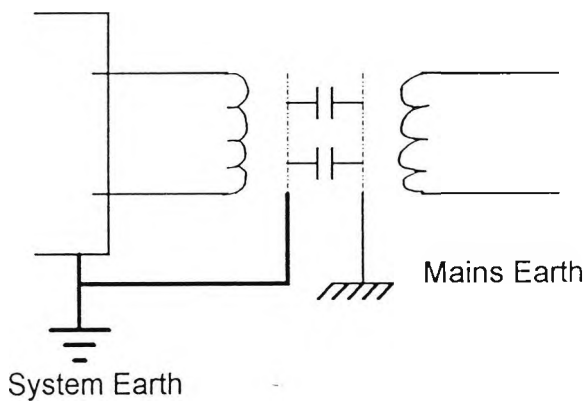


Figure 2.2 Capacitance between the screens of an isolating transformer

The operation of HV switchgear, HV breakdowns or HV sparks, the switching of inductive loads and fault currents give rise to intense broadband electric and magnetic fields as well as potential differences.

Screening of electric fields is achieved by use of a conducting screen. Screening of the magnetic component of the EM field is achieved by the use of a magnetic (Iron, steel) screen or a conducting (copper, aluminium) screen [Martin,1979]. In providing screening against EM interference (EMI), double screening is preferable around vulnerable equipment using metal enclosures. All edges must be joined and no apertures are allowed unless it is such that the interference is attenuated to insignificant levels after propagating through them.

The earthing of a screened room has no effect as far as the EMI is concerned, but it is of course necessary in respect of safety reasons and importantly in a substation or HV laboratory to provide safe electrostatic screening. This earthing must be done without creating an unnecessary ground loop.

2.4 Conventional Systems

Operation of traditional surge oscilloscopes in environments such as the HV laboratory was made relatively easy because of the level of SNR obtained with such systems. Surge oscilloscopes have input signals ranging up to 2 kV, whereas modern electronic instrumentations have signals which are three orders of magnitudes lower. This makes the achievement of an acceptable SNR for the modern system more difficult. Therefore preventive measures against interference due to EMI and ground loops are vital to the correct operation of the electronic instrumentation used in these circumstances. This calls for experienced and skilled staff and elaborately screened systems to ensure system operation with minimum interference and therefore acceptable measurement errors. A number of the 'conventional' transient recording systems which are used for impulse measurement in HV laboratories are discussed here:

Malewski describes a digital recorder for impulse measurement in an HV laboratory [Malewski, 1980] to replace the surge oscilloscopes which are traditionally used in HV environments. To protect the vulnerable electronics an electromagnetic shield was designed to house the ADC, the digital interface as well as the input attenuators. The attenuation of the HV signal to LV level required at the input of the ADC is carried out inside the enclosure to protect the low level input signal from interference. Isolating transformers and RF filters were used in the supply lines powering the instrumentation inside the enclosure. The terminal and the auxiliary display monitor are not protected by the high attenuation shield, the reason given being that their functions begin after HV impulse has elapsed and also because the keyboard and displays must be accessible to the operator.

In another report [Malewski and Poulin, 1985] a digital recording system is described for use for "finger print" transformer impulse testing. Transients involved in such tests do not have such steep wavefronts but since the "finger print" tests require the comparison of two records a relatively high measurement accuracy is required. The digitiser used in this recording system has a 10 bit resolution with a maximum sampling capability of 30 mega samples per second (MS/sec). Comparison between oscillograms and digital records are made and test results presented. The recording system used, however, suffered from interference which caused some discrepancies in the results obtained. Despite the careful design and manufacture of the digital recorder housing, the metallic conduits protecting the measuring cables and the voltage and current transducers, the shielding efficiency decreased at higher frequencies. Consequently the SNR started to decrease above about 2 MHz.

A digital Recording system for HV impulse measurement [Hausler, 1987] describes the careful measures taken to ensure the correct operation of the transient recorder in an electrically harsh environment. The entire transient recorder which includes the digitiser, the memory and control units are housed in a heavily screened enclosure to protect them from external interference. The trigger unit is also housed in the

enclosure and it receives its input from outside via a screened cable. The shield is reported to be designed against electric fields of up to 20 kV/m, magnetic fields of up to 60 A/m and currents on cable braids of up to 100 A. To ensure a good SNR, the input signal level to the recorder is +/- 1600V. This signal is then attenuated down for use for the ADC inside the enclosure so that external interference cannot degrade the reduced signal. In order to protect the system against any internal interference such as local ground loops and pickup, the recorder units are electrically isolated from the processing unit (the computer) by using optocouplers. Access to the CRO inside the enclosure is via coaxial cables. Although extensive measures were taken in this system against interference, it is vulnerable to large potential differences between the measured and the monitoring system.

An international collaboration on comparison of HV Impulse measuring systems, [McComb et al, 1989a] has been published reporting on the test procedures and results obtained. Four laboratories were involved in this collective work to produce recorded test results on their impulse voltage dividers compared to a resistance potential divider of agreed parameters and construction. The process of each test carried out in each laboratory and the measurement arrangement used is described. One of the aims of these tests was to ensure that each divider system was free from interference and proximity effects. Careful preventive measures were taken to reduce the effects of sources of errors as far as possible. The complete system was mounted on metallic sheets of aluminium or brass and single point grounding was used. The recording system was housed in a shielded enclosure which was supplied with AC power through isolating transformers and filters. In the case of the test arrangement at CERL, the signal cables were buried in the ground.

As mentioned earlier, identifying and controlling the ground loops could be a very complex process, but are vital in reducing their effects. However, the difficulty of the problem of identifying these ground loops becomes even more significant when measuring-system comparisons are carried out. The measurement could be carried out

under different 'conditions' of interference and ground loop arrangements for each laboratory and therefore there will be an uncertainty associated with each of the measurements. The response of the transfer system is determined not only by the transfer system itself but by its placement in the test circuit, i.e. lead length, grounding etc.

In [Shaw, 1989] a system is described to capture transients induced by lightning and electromagnetic pulse (EMP). Two digitisers were used: The Le Croy 6880 digitiser (1.35 GS/sec) and the 8828 digitiser (200 MS/sec). Special care was taken to eliminate magnetic coupling in any conductive loop formed by current and voltage metering cable shields. This problem can occur where shunt and voltage divider cables are fed to an instrument where the low side of the coaxial cables are common. This system is vulnerable to such ground loops problems as well as EM coupling. Fast transient signals, being rich in high frequency components, couple easily into cables and intermediate circuits. It was imperative to avoid such sources of error by using 'extensive' shielding provided by the shielded room and a totally enclosed metal test bay. Extra measures were also taken to ensure that the electronic instrumentation in the shielded enclosure operated satisfactorily. The mains supply to the electronic instrumentation within the shielded enclosure was supplied through isolating transformers and RF filters.

In [Lloyd et al, 1989] a system is presented for the recording of switching transients. Le Croy digitisers (8828) were used to capture switching transients and extensive measures were taken to prevent interference due to EMI and ground loops. Here again the computers and digitisers were installed in a shielded container as a protective measure against interference.

In [McEachern, 1990] a system is described for capturing and presenting short duration voltage surges on AC power lines. In this system the surge was sampled at a rate of 2 MS/sec and the resulting data is presented graphically. Printout data are presented; peak surge voltage, rise time, date and time of surge The author also

comments on the vulnerability of the system to surge pick-up by the instrument through the signal wiring. For correct operation, careful analysis of signal and instrument grounding is also emphasised; he comments on the conflict between conventional safety grounding and avoidance of ground loops through the instrument.

2.5 Optical Fibre Applications in H V and Power Systems

'Light'-based systems have features which make them attractive to many measurements and monitoring applications. The non-intrusive nature of fibre optic systems find useful application in field measurements. The second feature of the fibre optic systems is their inherent ability of providing electrical isolation while optically linking different parts of a circuit or a measurement system.

There have been numerous applications of optoelectronics and light communication in high voltage and power systems some of which are briefly indicated below.

The leakage current ratio detector described in [House and Lynch, 1984] consists of two "transmitter" units connected in series with the divider which is under test. The voltage drop across each resistor is applied to a voltage-to-frequency converter and the light from an LED is pulsed at the frequency so generated. The light is carried by optical fibres to the "receiver" unit in which the two frequencies are compared. To obtain a datum reading first the two transmitter units were connected in series at the earthed end of the divider, and the difference between their frequencies was observed for this equal-current condition. One of the transmitters was then transferred to the high-voltage end of the divider and the difference between the frequencies is again observed. Any change indicates how much of the current entering at the high-voltage end of the divider is leaking from it before reaching the low-voltage end.

A digital 300 kV electrostatic voltmeter [House et al, 1983] is built using a moiré fringe optical transducer in the voltmeter unit with optical fibres taking the signals to a remote indicating unit. The force due to the applied voltage turns a spindle unit against a restraining spring. The moiré fringe transducer responds to the movement and the

resulting changes in the diffraction patterns, monitored by 4 optical fibres, are remotely counted in an up/down counter to give the resultant deflection. To avoid having the light sources within the pressure vessel, the moiré fringe system is illuminated through a large optical fibre. The moiré system output data is processed at a remote location using a local microprocessor to give the calibrated voltage. The uncertainty of the calibration is reported to be +/- 1/3% of the full scale range (FSR), for voltages greater than one sixth of the FSR.

A paper [Esposti et al, 1987] describes a totally optical device for current measurements on a HV apparatus using a fibre optic sensor. In the device Faraday's Magneto-Optic effect is exploited in which the change of polarisation of a wave propagating through the fibre in the presence of a magnetic field is detected. A current range of 1-1000A for both DC and transient conditions is reported.

In [Sikorski, 1987] optoelectronics is used with air as the transmission medium instead of optical fibre. In this report, an optical link is used to transfer the firing impulse to the trigatron of the impulse generator. By this means expensive insulating impulse transformers or capacitors are eliminated and EMI problems are avoided.

A spherical electric field sensor [Feser and Gockenbach, 1986] is used together with an optical link for the measurement of transient electric fields and also High Voltage impulse measurement. The size of the sphere (8 cm dia.) is made small to cause minimum distortion of the field it is placed in [Feser and Pfaff, 1984]. An analogue link with a bandwidth of 25 MHz is used to communicate the data from the spherical sensor to a receiver unit. The sensitivity of the sensor is dependent on the position of the sensor with respect to the circuit / field.

A miniaturised space-potential DC electric field meter is reported in [Johnston and Kirkham, 1989]. The field meter is designed to measure the field under a DC transmission line in the presence of distorting objects. The meter uses a fibre optic cable to couple a small measuring probe to a remote 'readout' device, so as to

minimise field perturbation due to the presence of the probe. The electronics within the probe are powered by batteries fitted in the probe enclosure.

Further developments in the optical powering of remote transducers are reported in [Kirkham and Johnston, 1989; Adolfsson et al, 1989]. Electrical power is converted to optical power by means of laser diodes, and this is coupled into an optical fibre. At the transducer the optical energy is converted back to electrical power by means of photodiodes or photovoltaic converters. This removes the requirement of a battery supply in the remote sensor, but is only suited to applications in which the electronics of the sensor have a very low power consumption of around a few hundred μW. Higher power optical supplies are not practical because of the low power transmission efficiency obtained with present technology; at about 0.3% overall (electrical-to-electrical) [Kirkham and Johnston, 1989].

DC current measurement at high voltages is accomplished using Pockels cell and fibre optic links [Mitsui et al, 1987]. The Pockels effect has been exploited to measure electric field distribution on high voltage insulation systems by a number of researchers such as [Stringer, 1984; Huang and Erickson, 1989].

2.6 Optically Coupled Recorders

As with other light based measuring systems, optically coupled transient recorders designed for measurements in electrically harsh environments exploit the inherent properties of optical fibres for such applications. Optical fibres are immune to interference as compared to conductor cables. The coupling problems associated with coaxial links are non-existent as far as optical links are concerned. The extensive measures required to reduce the interference effects to negligible levels in conductor connected systems, are totally unnecessary for optically coupled systems. Another feature of the optical link which solves a different problem is the electrical isolation exhibited by the fibre allowing measurements to be made on systems at extremely high impulse AC or DC voltages. Different parts of a system linked by optical fibre will

have a complete galvanic isolation. This aspect is of a great advantage in avoiding multiple earth problems and therefore the difficulties of ground current loops which are common with conventional impulse measuring system. The optically coupled recording systems reviewed are classified in two categories: those using analogue fibre-optic links (FOLs) and those using digital ones. The systems using analogue links suffer from the non-linearity and signal distortion of such links which could result in additional error [Holden, 1993] in HV impulse measurements. The characteristics of the reported systems using digital FOLs make them unsuitable for HV impulse measurement; as will be seen from the review in the next section.

2.6.1 Recorders Using Analogue Links

An optically coupled HV measuring system is described in [Tempelaar and Koreman, 1983]. The output of a damped capacitive voltage divider (for voltage measurement) or that of Rogowski coil (for current measurement at high potential) is transmitted to a digitiser/recorder unit via fibre optic cables. The optical link is an analogue one having a bandwidth of 10 MHz. At the recorder unit, once the signal is digitised, data manipulation and processing are carried out by a computer connected to the digitiser, and the result is displayed on the monitor or plotted.

In [Miller et al, 1987] the fibre optic link is exploited for measurement of pulsed corona current on long horizontal conductor on air. In this work a high frequency current transformer is used to measure the transient waveform. This is coupled to a digital oscilloscope via an analogue fibre-optic link. The digital scope bandwidth is 20 MHz, with a maximum sampling rate of 100 MHz and the analogue fibre-optic system has a 50 MHz bandwidth. The fibre optic system is required to be calibrated before each measurement is carried out, because of the non-linear characteristics of the link.

In [Halkiadis et al, 1991] a fibre optic link is used for HV impulse measurement. The LV arm of the capacitive divider was coupled to a digital oscilloscope via an analogue

fibre optic link. The link had a bandwidth of about 35 MHz the maximum sampling rate of the scope was 400 MS/sec.

A report [Van der Sluis, 1989] published at the IEEE panel session describes an impulse measurement system which uses an analogue FOL to transmit the signal from the measurement to the recorder unit. The digitisation is accomplished at the recorder unit before the digital data is stored. Because of the non-linearity of the analogue FOL, the link had to be calibrated before each measurement. It was the conclusion of the author of this report that the analogue link was the 'weakest' part of the system, the performance of which seriously affected the accuracy of the measurement.

Commercial optically coupled systems using analogue links have also been reported to suffer from the drawbacks of non-linearity. In one case [Noe, 1993], it has been reported that the analogue link of the system suffers from non-linearity effects which resulted in unacceptable measurement errors. In another report [Holden, 1993], system response corrections were impossible to achieve because of the non-linear characteristics of the analogue link used in the impulse measurement system.

2.6.2 Recorders Using Digital Links

Dyer and Holbrook [1986] report on an optical link which was developed to interconnect a Tektronix sampling head with its plug-in unit in a Tektronix time domain reflectometer (TDR) unit. The latter is installed in the plug-in bay of a Tektronix 7000-series main frame sampling oscilloscope. The sampling head was placed in the noisy environment where the measurement took place and relayed the information via data links to the sampling oscilloscope mainframe where the measured signal was displayed. The optical link consisted of three channels; the error link, the feedback link and the strobe link. These are the normal communication channels between the sampling head and the TDR unit of the conventional oscilloscopes. Essentially, this investigation replaces the three conventional (conductor-connected) links with optical fibres. The Tektronix sampling head is reported to be capable of

measuring repetitive signals with up to 6 GHz bandwidth. This system, therefore cannot be used for single-shot applications because the sampling technique requires a repetitive signal. The error and feedback links have bandwidths of 270 KHz and 4 KHz respectively.

Murphy [1990] reports on an optically coupled transient recorder that is designed for unattended recording of lightning induced voltage surges for extended periods of up to one year. This objective was met by using devices that have very low power consumption and that the recorder is only activated in the presence of a surge. In the presence of a signal it took up to 6 μs for the power supply to the electronics to stabilise and the ADC to initiate data acquisition after the input signal exceeds the pre-set levels of the detector. The ADC has a 7-bit resolution and operates at 5 MS/sec. The system was used to formulate a data base of lightning events.

2.7 Digital Optically Coupled Transient Recorder

Accurate measurement of HV impulses entails overcoming many problems associated noisy environments such as the HV laboratory. Over the last decade there has been much effort put into digital recording of HV impulses [Malewski, 1980; Van der Sluis, 1989]. The use of optical connection between the HV circuit under test and the monitoring equipment overcomes the difficulties associated with potential difference due to ground loop currents. However, although with the use of optical connection many of the preventive measures required in conventional HV system may be dispensed with, there still could be subtle sources of error associated with optical connections.

Optical fibres are insensitive to EM interference in terms of induced voltages and therefore the signal being transmitted through the fibre is said to be immune to such interference. However, optical fibres react with magnetic fields resulting in such effects as the Faraday's magneto-optic effect which causes the rotation of polarisation of light propagating through the fibre. As far as the signal being transmitted through the fibre

is concerned, this causes phase changes and therefore distortion in the signal. An analogue FOL may be directly vulnerable to such interference whereas a digital FOL is not susceptible to such effects except in extreme cases. Any changes in polarisation due to EM field appears as phase-changes or signal distortion but these polarisation effects are small. For a digital link, on the other hand, the same polarisation effects would not result in error in the detection of data since in the binary system of the digital link such effects would not cause a '1' changing to a '0' or vice versa. Strong EM fields are produced when HV breakdown occurs or impulses are generated or chopped. When such transients are to be recorded, in the presence of such fields, the measurement accuracy of recorders using analogue FOL, will be undermined because of the EM fields' distorting effect on the signal being recorded at that instance. Apart from the vulnerability of analogue FOL to polarisation, they are also subject to non-linearity effects which must be taken into account prior to measurement. The performance of analogue links are directly influenced by the characteristics of the optical cable as well as those of the optical source and detector.

To summarise, analogue FOLs are subject to non-linearity effects, as well as ageing and temperature effects, all of which result in signal distortion and therefore measurement error. The fibre may also be susceptible to polarisation change due to EM fields and mechanical strain. These may be effectively eliminated by digitising the signal at source before transmitting the information for recording.

In this work an impulse measurement system is proposed in which sources of error associated with optically coupled systems using analogue links are avoided. This system consists of two parts; the capture unit and the recorder unit, interconnected by a digital FOL. In this system, the digitisation of the signal being monitored is accomplished at 'source', the measurement point, before transmitting the digital data to the recorder unit for storage and processing.

Digital recording of HV impulses must be carried out with minimum introduction of error. In any digital measuring system, one of the sources of error as far as the

measurement accuracy is concerned is that of the digitiser. In an optically coupled system using an analogue link and in all such systems reviewed here, in the addition to the digitiser used at the recorder unit, the analogue FOL is the second source of error within the system.

In the DOCTR system the source of error due to the analogue FOL is avoided by the use of a digital FOL between the two parts of the system. In contrast to the analogue FOL the performance of the digital FOL is less susceptible to any non-linear characteristics of the optical source and detector in the link. In addition it is also insensitive to changes in the characteristics of the optical fibre cable due to mechanical strains, intentionally or unintentionally applied on the fibre. With the digital FOL providing a linear channel of communications, in addition to the linear characteristics of the recorder unit, the resolution and accuracy of the digitiser will determine the uncertainty of the measurements

Another concept which is crucial in HV impulse measurements is the need to be able to produce traceable measurements. Impulse recording systems using digital FOLs allow a more reliable measurement compared to those using analogue links. This enables the DOCTR system to achieve traceable measurements of good accuracy with comparative simplicity.

The capture unit consists of a flash ADC and the transmitter end of the FOL shielded in a copper box together with the battery and supply regulating monitoring circuits. The recorder unit includes the receiver end of the FOL, the RAM bank and associated control circuit, the interface between the recorder unit and a standard PC. The FOL is made up of nine parallel channels each capable of transmission rate of more than 300 Mbit/s.

The system has a sampling rate of 100 MS/s. For single shot applications of HV impulse measurement, this real time recording of data is limited, at the present state of technological development; only by the ability to store it directly in high speed RAMs.

Random transients may be captured by this system since an external trigger is not required for the system. The number of pre-event samples and the level at which recorder is "triggered" may be programmed by the user.

The capture unit, which is screened against EM interference may function in electrically harsh environments whereas the recorder unit could operate in a relatively interference-free area. The small size of the capture unit provides access to parts of the HV circuit where space is limited. The capture unit can monitor signals at high-potential elements of the HV circuit and communicate its output to the recorder unit on ground potential. This is because the electrical isolation between the two units of such a recording system, provided by the FOL, avoids the problems associated with the potential differences and those due to common ground circuits.

2.8 Summary

The typical measurement difficulties encountered in hostile EM environments have been presented and the preventive measures taken to reduce their effect when using 'conventional' instrumentation outlined. These laborious steps may be overcome by using 'light' based systems which enjoy the electrical isolation of the optical fibre and its excellent EM noise rejection property. However the non-linear features of analogue FOLs could undermine the measurement accuracy. A review was presented of the conventional systems used for HV impulse measurement. This was followed by a review of systems for measurement in electrically harsh conditions. These systems were grouped into two categories: analogue and digital systems. The analogue FOL systems, although they had a very wide bandwidth, suffered significantly from non-linearity effects to the degree that the results obtained were reported to be unsatisfactory. Analogue fibre optic links are particularly vulnerable to changes in the characteristics of the optical source and detector as well that of the optical cable. The only digital system reported was at low speed which is inadequate for fast impulse measurement. The system proposed in this work uses a digital link and its speed of operation meets that required for HV impulse measurement. Digital links are far less

susceptible to changes in characteristics of the optical components of the link or the latter's non-linear performance. In the next three chapters the main units of the DOCTR system are discussed starting with the digitiser in the following chapter.

CHAPTER 3

ANALOGUE TO DIGITAL CONVERSION

3.1 Introduction

The widespread application of digital computers and other digital information-processing tools has produced a growing requirement for better devices for the conversion of information from "natural" sources to the digital domain. There are numerous benefits in adopting a digital representation for information-bearing signals [Aaron, 1979]. Digital signals are less susceptible to transmission noise and are easier to store. The processes of transmission and switching of information are unified in the digital domain. Furthermore, fast and complex signal processing techniques are applicable to digital signals.

Most sources of information are, however, analogue in nature in that the signal waveform assumes a continuum of values in time and amplitude.

The devices used for converting information from the analogue domain to a digital representation are referred to as Waveform Encoders or Analogue-to-Digital converters (ADCs).

Digital recording techniques open new possibilities for the recording of the results from high voltage impulse testing.

In this chapter the principles of analogue to digital conversion are considered and the various conversion techniques and architectures are briefly outlined. The accuracy limitations and the linearity of the analogue-to-conversion converters (ADCs) are considered. The effect of oversampling and the reduction of noise are also discussed. The relationship between the sampling rate of the digitiser and the accuracy of the impulse measurement are also discussed.

3.2 Analogue-to-Digital Conversion

Waveform encoding can be regarded as consisting of the two commutable processes of sampling and quantisation corresponding to time and amplitude discretisation. The quantisation process is here taken to include coding for the digital representation of the signal. While time sampling of signals can be achieved without loss of information, the quantisation process is an irreversible, information lossy process. The quality of analogue-to-digital converter devices depends on how close the quantised samples are to the analogue input samples. In general, this will be a function of the number of discrete levels that the ADC can assume and also of the accuracy with which the discrete levels are selected . The number of ADC levels is $N=2^n$ where n is referred to as the number of bits of resolution of the converter. To minimise the loss of information due to the conversion process, it is desirable to maximise n, given that all other parameters remain constant. The other performance measure for waveform converters is the conversion rate. This reflects the maximum bandwidth of the input

analogue signal that can be converted without significant loss of information introduced by the sampling process.

Practical difficulties are faced as the number of bits is increased. At present linear electronic ADCs can have up to 20 bits resolution at audio frequencies [Analog Devices, 1992]. This increase in resolution is traded off with a corresponding decrease in conversion rate. On the other extreme, ADCs may be designed to operate at very high conversion rates, but at the cost of lower resolution. This is because improvement in performance requires an increase in the precision of the analogue circuits as well as an increase in the number of internal components. The required degree of component tolerance rises with resolution as a factor of n. The close tolerance required for state-of-the-art performance are difficult to obtain and to maintain over time and temperature variations. ADCs have been reported of being capable of 500 MS/s but at a nominal 8 bit resolution [Schiller and Byrne, 1991]. Signal processing is used to enhance the resolution of the converter while operating several ADCs in an interleaving mode to increase the effective conversion rate. In [Schiller and Byrne, 1991] eight of the reported ADCs are interleaved to achieve an effective conversion rate of 4 GS/s.

3.3 Waveform Encoding Principles

In this section the two main operations of *sampling* and *quantisation* are discussed and their contribution to the overall quality of the conversion process is presented.

3.3.1 Sampling

Sampling a continuous waveform is the first step in the process of conversion to the digital domain. Signal samples are measures of amplitude evaluated over short time periods. This period should be so short as to make the signal changes which occur within it insignificant. The sampling process can be regarded as a switching operation. An ideally-sampled signal can therefore be regarded as a train of impulses, with the amplitude of the continuous input at the sampling instant.

According to the sampling theorem, a signal having no spectral components above f_o can be determined by its samples at uniform intervals spaced no more than $1/(2f_o)$ apart [Nyquist, 1928]. The spectrum of the sampled signal is the same as that of the continuous waveform, repeating itself periodically at multiples of the sampling frequency (Fig 3.1). The original signal can be retrieved by a low pass filter. If the sampling frequency $f_s < 2f_o$ an overlap of adjacent spectral segments results, causing the distortion known as aliasing.

3.3.2 Quantisation

Quantisation is the process of mapping the continuous input amplitudes to discrete sets of output amplitudes known as quantisation levels.

Fig. 3.2 shows the transfer characteristics of an ideal uniform quantizer. The signal amplitude x may fall in one of the quantization intervals.

$$t_k < x \leq t_{k+1} \tag{3.1}$$

The output levels Y_k are referred to as the quantisation levels. For uniform quantization we have

$$Y_{k+1} - Y_k = q \tag{3.2}$$

$$t_{k+1} - t_k = t_s \tag{3.3}$$

Where q is referred to as the quantizer step size. The quantizer characteristic shown in Fig 3.2a is known as "mid-riser". This is because zero is not one of its output values. For "mid-tread" quantizers, shown in Fig 3.2b, one of the output levels, q_k is zero.

Unlike the mid-riser characteristics, the mid-tread characteristics gives an output which is insensitive to infinitesimal input changes about zero and is therefore generally preferred. Both characteristics introduce a maximum error of 0.5 q.

It can be shown that the inherent quantization error, or noise, is given by its rms value:

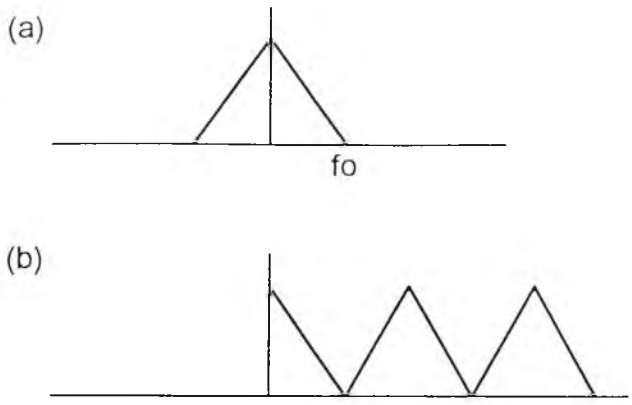
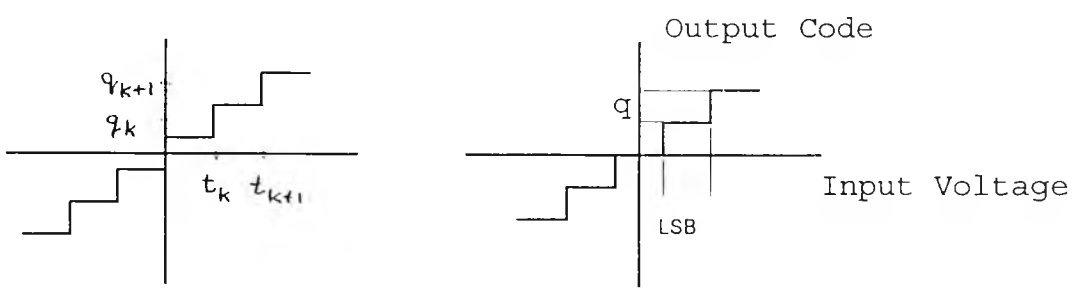


Figure 3.1 Spectrum of (a) Analogue signal (b) Sampled signal



(a) Mid-riser (b) Mid-tread

Figure 3.2 Mid-riser and Mid-tread characteristics

$$Q_n = q / \sqrt{12} \qquad (3.4)$$

This quantization noise results from the difference between the quantized signal and the analogue continuous signal, and its peaks remain within +/- 0.5 q .

The quantization error waveform has a spectrum that is low pass and much wider than the input signal spectrum [Bennett, 1948]. Sampling of the quantized signal, being equivalent to the quantization of a sampled signal, causes the aliasing of the quantization noise spectrum. As a result of the folding of the quantization spectrum segments into the baseband, the noise spectrum flattens.

3.4 Conversion Techniques

There are numerous architectures for analogue-to-digital converters and many more specific circuit designs [Gordon, 1978]. In this section the basic operation of the parallel converter is described, which has the fastest conversion rate amongst the linear electronic ADCs. Other converters which use different architecture and technology, such as the Electron-Bombarded Semiconductor (EBS) and the Scan converters have a conversion rate higher than the parallel ADCs. The above converters are not used in this work because of their size but will introduced later in this chapter.

3.4.1 Parallel Converters

Parallel or "flash" converters use a resistor chain and a set of comparators to establish quantization thresholds and to find the quantum associated with input level. The output of the comparators is then coded to provide binary output. The advantage of flash converters is that conversion occurs in parallel and the conversion speed is limited only by the delay within the comparators and gates which results in very fast conversions. The drawback is the exponential rise in the number of components required as the resolution increases.

3.4.2 Alternative Conversion Techniques

The need for high performance converters in instrumentation and waveform acquisition has led to alternatives to the conventional circuit approaches to improving converter performance. All these techniques involve trading off speed to achieve higher resolution and / or accuracy. In some techniques oversampling is used in the conversion process. Oversampling implies that the input to the conversion system is sampled at higher than the Nyquist rate. One example of oversampling schemes is the stochastic technique of adding a pseudo-random noise signal to the oversampled input before quantization and averaging the digital output. Such so called "dither" signals provide a means of achieving resolution below the least significant bit of the internal quantiser [Vanderkooy and Lipshitz 1984].

Feedback conversion systems provide an alternative means of producing the intermediate code in oversampled systems. Predictive and noise-shaping coders, such as delta modulators, sigma-delta modulators and interpolative coders employ feedback to reduce the in-band quantization noise [Tewksbury and Hallock, 1978]. Interpolation technique is another converter architectural approach to attain higher resolution ADCs.

Two other techniques used at ADC system level to achieve higher resolution and effective sampling rate are; subranging and interleaving . The subranging technique is used to produce a higher resolution ADC using two lower resolution ADCs and a DAC. The input signal is digitised by the first ADC and its digital output is fed into a DAC. The output of the DAC is subtracted from the delayed input signal and the residue is fed into the second ADC to give a higher overall resolution

The interleaving technique is used to enhance the effective sampling rate of the signal digitised. At least two ADCs are used in this method both of which are driven by the same sampling clock but at different phases of the clock signal. In the case of two ADCs working in interleaving mode, the clock phases driving them are 180 degrees out of phase with respect to each other and the effective sampling rate of the complete converter unit is twice that of the individual ADCs used in this system or the of clock

frequency [Fig. 3.3]. More than two ADCs may be used in interleaved mode but clock synchronisation for individual ADCs become critical and more difficult as the number of ADCs is increased. For example for three ADCs used in interleaved mode the phase difference of the clock signals driving the individual units will be 120 degrees and in the case of four ADCs used in interleaved mode this difference will be 90 degrees. The effective sampling rate of these interleaved systems will be three and four times the clock frequency driving each system respectively.

3.4.3 Oversampling

From the Nyquist theorem it is clear that, ideally, a sampling frequency of twice the bandwidth is sufficient for distortion-free coding of the signal. The term "oversampling" refers to sampling a signal at a frequency greater than twice its bandwidth prior to uniform quantization. The effect of oversampling a signal prior to uniform quantisation has been studied by Bennett [Bennett 1948]. By considering the quantisation of this input signal prior to its sampling, he was able to derive analytical results for the output auto correlation and the noise power spectral density. In addition he also computed the spectrum of a quantised signal.

If the signal is sampled at twice the input bandwidth, the quantisation noise spectrum is aliased back into the base-band giving rise to a total noise power of q^2 / 12. As the sampling rate is increased by a factor of two, the in-band noise power drops by approximately 3 dBs. This is because the quantisation noise is now spread over twice the frequency range. However, at very high oversampling rates a limit is reached, given by the inherent total in-band noise of the quantiser prior to sampling. For an 8-bit converter, this limit is reached when the ratio of the sampling rate to the input signal frequency is about 400 [Bennett, 1948]. It can be seen therefore, that a reduction in quantization noise can be achieved by operating the ADC at a higher speed.

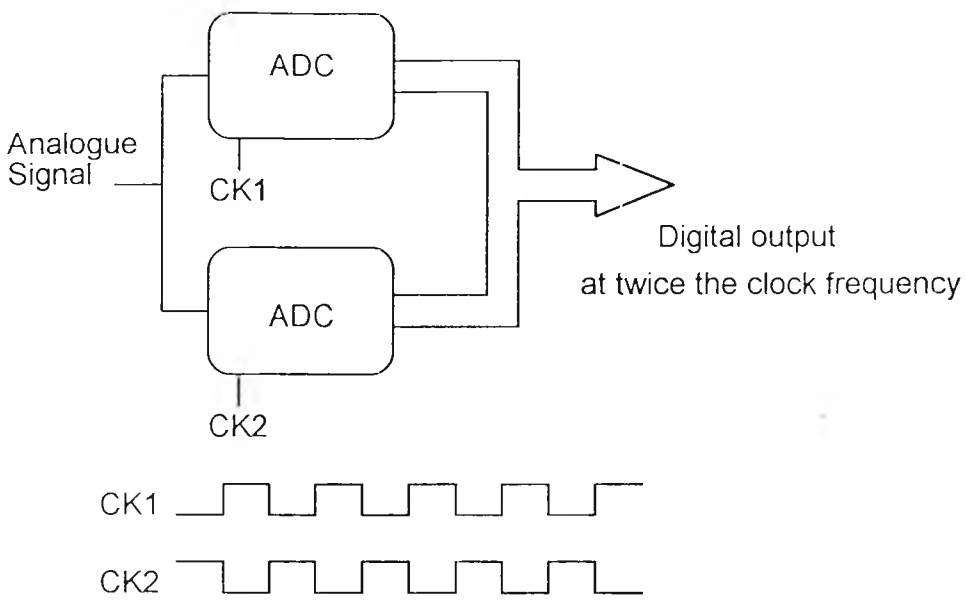


Figure 3.3 Interleaving techniqes using two ADCs

In addition the total amount of noise reduction achievable increases with the number of bits in the quantizer. In fact for every one-bit increase in the quantiser resolution, the SNR is enhanced by 6 dBs.

3.5 Accuracy Limitation of ADCs

An ideal uniform converter has an input /output characteristics similar to those shown in Fig 3.2b. In particular, the threshold values are precisely defined, uniformly spaced and are stable over time and temperature variation. The quantisation levels, defined by the threshold position, are also uniformly spaced and stable.

Practical ADCs, however, suffer from a finite amount of non-linearity. This non-linearity presents itself as static and time-varying deviation in the position of the quantiser thresholds from the ideal. These errors are in addition to gain and offset errors in the ADC and aperture errors associated with sampling. The non-linearity errors however, are more significant than gain and offset errors which can be easily corrected.

Numerous sources contribute to the presence of linearity errors in the ADCs during the manufacturing process. In practice, it is impossible to eliminate these errors altogether but, techniques such as laser trimming can be used to reduce the static linearity errors to specified levels. The effects of linearity errors on ADC performance are considered in this section.

3.5.1 Gain and Offset Error

Both gain and offset errors in a converter result in the coding range not being fully used, and lead to an increase in the quantisation noise. With gain error a rotation of the ideal characteristic takes place about the zero input level. In the case of offset error, there is a shift of the entire transfer function with all points equally affected. This leads to an overload characteristic which is asymmetric, and therefore a loss of input signal range will occur.

Most converters have external means for the adjustment of gain and offset. This will allow any drift of these parameters with time to be corrected. At near-constant temperatures, drift remains small and calibration at the operating temperatures is usually sufficient.

3.5.2 Linearity Errors

The line joining the midpoint between threshold levels on the ADC characteristic is a straight line for ideal converters. Gain and offset errors do not alter this and while noise in the quantizer may make the line fuzzy, its mean will still be straight. However, if the threshold levels are not equally spaced this will cause a deviation from the straight line.

The terms linearity and non-linearity are somewhat imprecise and manufacturers specification of these features reflect a lack of clarity. However, there have been attempts to produce a consistent terminology and set of definitions in this area [Tewksbury et al, 1978]. Here some of the important terms which are relevant to this work are defined.

"Linearity" refers to the extent to which the actual static transfer characteristic follows a straight line, while "non-linearity" describes the deviation from this ideal. The two main measures of linearity are the differential linearity error (DLE) and the integral linearity error (ILE). The integral linearity error, sometimes simply referred to as linearity error, is the deviation between actual and ideal quantisation levels. The differential linearity error is the difference between actual and ideal separation of adjacent levels. These two measures can be evaluated at each quantisation level throughout the coding range. However, in manufacturers specifications of linearity and differential linearity, the maximum value across the entire coding range is quoted.

Good quality converters have linearity errors specified to +/- 0.5 LSB for both ILE and DLE. When the DLE is greater than +/- 1 LSB the output of the ADC will exhibit

missing codes while a DLE which is less than +/- 1 LSB ensures that no codes are missing.

The other linearity measures, related to threshold position in the ADC, are those which describe absolute and relative accuracy. Absolute accuracy is the worst-case difference between the actual and ideal threshold levels. This is a strong function of the gain and offset errors of the converter. Absolute accuracy measurements are made under a set of standard conditions with sources and meters traceable to an internationally accepted standard. "Relative accuracy" is the worst-case difference between actual and ideal threshold levels after the full-scale range has been calibrated i.e. the full-scale range is adjusted to eliminate the gain and offset errors.

The accuracy of threshold position determines the position of quantization levels from which the linearity error measures are computed.

It is important to note that the maximum DLE and ILE are measures of static linearity performance.

Describing the performance of converter under dynamic conditions is difficult as there is no single, well-defined time-varying signal that accurately models the operating condition of the converter. However, the static transfer characteristics is a valid model for the converter with input signals confined to some frequency range specified by the manufacturers.

3.5.3 ADC Errors

It can be shown that the signal-to-noise ratio (SNR) for an ideal converter is given by:

$$SNR = 6.02n + 1.76 \text{ dB} \qquad (3.5)$$

The noise includes all non-fundamental spectral components which in a non-ideal converter would include the harmonics and any spurious frequencies but excluding DC.

The only noise source in an ideal converter is the quantization noise which may be expressed by its rms value as:

$$Q_n = q / \sqrt{12} \qquad (3.6)$$

where $q = LSB$

It is clear that as the resolution of the converter is increased, the quantization noise is reduced accordingly and this has the effect of enhancing the SNR. In fact for a 1-bit increase, there is a 6 dB gain in the SNR. The SNR is also dependent on the ratio of sampling speed to input frequency which increases at a rate of 3 dB per octave [Bennet, 1948].

Any component tolerances which result in imperfect performance of the converter are not taken into account in the above equation. Errors due to such effects are known as linearity errors or harmonic distortion which will be discussed later in this section. The above equation (3.6) also assumes that the converter is excited by the input signal to its full scale range (FSR). The noise level is increased if the input signal amplitude does not span the entire input range. This may be accounted for in the above equation as given by:

$$SNR = 6.02n + 1.76 - 20 \log \{ FSR / \text{actual input amplitude} \} \text{ dB} \qquad (3.7)$$

Traditionally, the SNR referred to the signal being the fundamental frequency and the noise any thing unwanted; such as harmonics, spurious frequencies etc. However, it is important to determine if the SNR specified is with or without distortion. The signal-to-noise ratio and distortion (SINAD) may be calculated if the SNR without distortion and the total harmonics distortion are known, as given by:

$$SINAD = -10 \log [10^{-SNR/10} + 10^{THD/10}] \qquad (3.8)$$

The total harmonic distortion (THD) is the ratio of the rms sum of the harmonics to the rms sum of the fundamental signal. The harmonics appear at integer multiples of

the fundamental frequency. Integral non-linearities appear as harmonics in the frequency domain. In practice the first five harmonics are the major contributors to THD.

3.5.4 Hysteresis and Noise

Quantizer hysteresis is due to storage effects within the physical converter devices. As a result of the hysteresis, output samples become dependent not only on the input samples, but also on the preceding outputs.

Another important imperfection in practical ADCs is the presence of input noise. This includes noise generated in the converter from sources such as comparators, resistors etc. Also, noise can be coupled-in from the power supply or surroundings. Even when all external noise sources have been eliminated, there is the unavoidable thermal noise due to resistive components which sets the theoretical minimum noise level for ADCs. In practice other sources of noise are much more significant.

3.6 Linearity Performance of ADCs

The full relationship between ADC non-linearity and the fidelity of converted signals is complex. In general, the presence of linearity error is a cause of distortions in the conversion process, although the exact nature of these depends on the detailed characteristics of the non-linearities.

The deviation of the quantizer threshold levels from their nominal positions, in general, partly random and partly systematic.

As a first approximation, the total ADC error power can be considered to have two components, one due to quantization noise, N_q, and the other due to the inaccurate position of threshold levels, N_a. The total noise, N_t, can then be written as,

$$Nt = Na + Nq \qquad (3.9)$$

For a high-accuracy converter N_a can be assumed to be negligible and

$$N_t = N_q = q^2 / 12 \qquad (3.10)$$

An n-bit converter with +/- 0.5 LSB DLE is considered to be n-bit linear. For larger linearity errors, the converter can be considered to be equivalent to an ideal converter with lower resolution, m such that

$$N_a^n + N_q^n = N_q^m \qquad (3.11)$$

When the linearity errors have a systematic component, a simple analysis such as that presented above is inadequate.

The auto-correlation function of the integral and differential linearity error data can be used to reveal spatial correlation between error magnitudes. This approach can be used to reveal the random, periodic and aperiodic components of the linearity error [Kuboki et al, 1982]. It is also possible to investigate the periodicities in the linearity error data using transform domain techniques [Bossche et al, 1986]. A general analytical treatment is often impossible and there is a need for computer simulations to study the effect of particular linearity error on the performance of the conversion system. Many studies have been made to investigate the effect of such errors on digitisers used in HV impulse measurement applications. These will be referred to later in the chapter.

3.6.1 Flash ADCs

Flash converters do not usually show periodic structures in the linearity signatures. This is because of the natural independence of the comparators in the conversion process. Defects in the manufacturing process can, however, lead to random and systematic errors in the transfer characteristic of these converters. Aperture effects are a limiting mechanism for flash converters and contribute to both wide-band noise and harmonic distortion. As the input signal frequency is increased, the finite "aperture time" of the converters may lead to slew-rate limitations. Variations in the sample duration and lack of conversion synchronism between the comparators could also lead to the introduction of wide-band noise in the spectrum. ADC input bandwidth and

sampling rate are usually specified by the manufacturers to limit the effect of these errors to within +/- 0.5 LSB.

3.7 Measurement of Linearity

There are two main approaches to the measurement of ADC linearity: static and dynamic tests. These differ in the frequency of the test signal used to excite the device under test. While in static tests a DC or low-frequency excitation is used, dynamic tests utilise input signals which contain high-frequency components. Dynamic performance tests are able to show up error mechanisms that come into play in realistic operational situations. The performance of the ADC is not constant at all input frequencies as effects such as aperture uncertainty and slew rate limitations are frequency-dependent phenomena. However it is difficult to find a test signal which is adequate in characterising the device under all its operating conditions [Tewksbury et al,1978].

It is often necessary to make a range of static and dynamic tests to establish the limitations of any particular device.

3.7.1 Servo-loop Test

A simple test technique for the measurement of the static linearity of converters is based on the measurement of each quantization threshold [Corcoran et al, 1975]. This technique which is sometimes referred to as the "servo-loop" test, is employed to obtain the static linearity characteristics of ADCs.

3.7.2 Histogram Testing

The histogram, or code density test is a means of characterising the ADC in the amplitude domain. This is achieved by using a sine wave excitation and accumulating a histogram of the output codes [Plessey, 1988].

A full scale sine-wave is used in order to exercise all the codes and to subject the converter to the maximum slew-rate at the chosen frequency. The choice of the input frequency is of great importance. Because the test is based on the random sampling of

the sine-wave, it is required that the sine-wave frequency should be non-coherent with the sampling.

It is impossible to measure the gain and offset errors as well as the DLE and ILE [Doernberg et al, 1984]. However a large number of samples is required for accurate computation of the linearity performance. In the case of a 12-bit converter, for 99% confidence and 0.10 bit precision in the DLE measurements, 4.2 million samples are needed. To estimate the ILE with the same precision, much larger record is required and the testing time is significantly increased [Doernberg et al, 1984]. This makes tests much more sensitive to drifts in the device and to the input source amplitude, with the resultant possible errors. The FFT test, however, is not sensitive to the problems as it requires very few samples in comparison.

3.7.3 FFT Testing

The Discrete Fourier Transform (DFT) of the ADC output provides an estimate of its spectral content. When the input to the ADC is a sine-wave, such a discrete spectral estimate can provide information about the linearity errors in the ADC. Also other performance evaluations such as SNR and THD can be estimated from the spectrum. When the transform is performed using one of the fast algorithms developed for its computation [Brigham, 1974] it is referred to as the Fast Fourier Transform (FFT) test. The FFT test is a means of characterising the ADC in the frequency domain [Plessey, 1988].

3.8 Impulse Digitisation

The need to "capture" non-repetitive, "single-shot" transients prompted the development of high writing speed cathode ray tubes (CRT). The transient waveform was then recorded using a camera and the resulting oscillogram was used for further analysis, comparison and storage. For digital analysis a CRO-TV camera hybrid system was developed in which the transient was "written", at high speed, on a temporary target and then the record could be scanned at a slower pace for analysis and storage.

The modern equivalent of CRT type digitisers are the scan converters which are capable of equivalent sampling rates of 100GS/s [Tektronix,1984]. This is faster than any modern electronic ADC, but the latter is much more compact than the former. On speed performance basis, however, recent advances in fabrication technology and with the introduction of new sampling methodology, have resulted in converters with relatively higher sampling speeds of 500 MS/s [Schiller and Byrne, 1991]. An interleaved system of converters is now capable of delivering a sampling rate of 4 GS/s.

Scan converters are physically bulkier and have greater power supply requirements than ADCs. This makes the scan converter less desirable for the application of this system in which the converter is housed in one-half of the system i.e. in the capture unit, operating on battery supply. The physical dimension of the digitiser systems based on scan converters (such as the Tektronix 7912) makes them unsuitable for applications which this system is intended for. In fact the dissatisfaction of researchers with such a system in the field of measurement in harsh environments, inspired this present work. In this system "flash" ADCs, which are the fastest type of non-scan converters, are used to capture the transient signal.

3.8.1 Relationship Between Accuracy of Peak Measurement and Bit Resolution

In this section, the requirements that a digitiser must meet for single shot HV applications are considered given the time and amplitude accuracies to be achieved according to international standards. Impulse digitisers must meet the accuracy requirements of 2% in amplitude and 4% in time measurements [IEC790,11984]. The 4% accuracy for a 500 ns impulse measurements corresponds to a minimum sampling limit of 50 MS/s. This means that the smallest time interval that can be resolved is 20 ns.

In amplitude measurements there are two criteria that have to be met which particularly apply to HV impulse measurement. One is the accuracy achieved in peak

voltage measurement of chopped impulses. If a ramp which collapses instantaneously is considered (Fig 3.4), the maximum possible error that can occur, around its peak, when digitised at a rate of one sample every t_S time unit is given by

$$E_m = m_r \cdot t_S \qquad (3.12)$$

where m_r is the slope of the ramp and $t_S = 1/f_S$ where f_S is the sampling frequency.

The magnitude of the maximum error, or the accuracy of peak measurement therefore depends on both the rate of rise of the impulse and the sampling rate

A maximum inaccuracy of 2% in peak voltage measurement (an error of 5.1 LSB for an 8-bit converter) corresponds to a given maximum rate of rise. Usually flash ADCs with 8-bit resolution have a linearity error of +/-0.5 LSB. This indicates that samples taken at areas other than the peak region of the impulse are digitised with an accuracy of +/-0.5 LSB while those around a peak region could be subject to an uncertainty of up to 10 fold greater. It is interesting to note that in order to achieve a +/-0.5 LSB accuracy at this rate of rise, the sampling rate would have to be increased tenfold. This would corresponds to an accuracy of 0.2%.

Needless to say that such an impulse, considered above, is ideal and in practice the rate of fall of the collapsed voltage is finite and not instantaneous. In addition, the size and therefore the response of the HV circuit has the effect of rounding the edges of the chopped impulse. These factors tend to make the magnitude of the error at the peak smaller than the maximum error achieved from the hypothetical impulse and therefore result in lower peak measurement error.

The other criterion which the digitiser must meet is that any superimposed frequency, which manifests itself as a 'kink' on the wavefront, has to be resolved. The maximum frequency of oscillation is dependent on the size of the HV circuit, with larger circuits producing lower oscillations [IEC60, 1973] The impulse generator used at the City

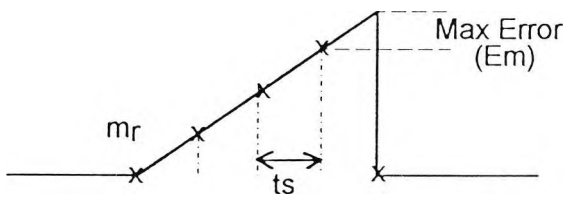


Figure 3.4 Chopped waveform showing worst-case sampling instances

University HV laboratory is capable of about 2 MV impulse generation, corresponding to a maximum oscillation frequency of 5 MHz according to this standard.

The effect of sampling causes distortion in amplitude which is referred to here as simply amplitude error. The magnitude of the amplitude error due to sampling depends on the ratio of sampling rate to maximum frequency of the signal being digitised. For a sinusoid of frequency f, the amplitude error is given by: [McComb et al, 1990]

$$1 - \cos(\pi / n) \qquad (3.13)$$

where n in this case is f_s / f or the number of samples per cycle

In the limit of large number of samples/cycle the error approaches zero.

In order to resolve the frequency of oscillation superimposed on the waveform with an accuracy of 2%, the ratio of sampling rate to frequency must be at least 15 (n=15 in equation 3.13). For an oscillation frequency of 5 MHz, the sampling rate must therefore be 75 MS/s.

The ADC used in this system has 8-bit resolution operating at 110 MS/s. This is double the rate required for impulse measurement which also exceeds the sample speed required to resolve superimposed oscillations at 2%.

Over the last ten years there have been numerous and concerted effort by researchers in characterising digitisers for High Voltage Impulse measurements. Various experimental procedures have been devised and analytical methods suggested for studying the behaviour of impulse digitisers.

Dynamic performance is one of the behaviours of the impulse digitisers which have been investigated for different digitisers by many researchers with interest in HV impulse measurement [Malewski, 1983; Peetz, 1983; Schon, 1983; Kuffel et al, 1986; McComb, 1987; McComb, 1989b; Kuffel, 1989].

Computer simulations of dynamic performance of impulse digitisers are also used to investigate the behaviour of such digitisers in response to increasing input signal steepness[Kuffel et al, 1991].

The unit step response of impulse digitisers have also been studied and test methods proposed by a number of researchers [Schoenwetter, 1984; McComb, 1991].

The effective bit (EB) resolution of digitisers tend to reduce at high input signal frequency compared to the nominal figure at DC or low frequency. Since the behaviour of the impulse digitiser is of particular interest for high frequency input signal, the EB resolution has also been investigated [Kuffel, 1987; McComb, 1989c].

Differential linearity performance of a digitiser is a fundamental measure of its performance. Differential linearity errors of a digitiser are of particular interest at high input signal and clock frequencies. DLE test also reveal errors which are not shown explicitly by other tests [McComb et al, 1987].

3.9 Summary

The different types of digitisers were considered with emphasis on those most suitable for measurement of steep-fronted impulses. The various sources of errors which are significant in impulse measurement were discussed. Also the relationship between the rate of rise of an impulse amplitude and the sampling rate of the digitiser were considered. The accuracy of peak voltage measurement was considered and the evaluation of the sampling rate which would give uniform accuracy throughout the impulse waveform was presented.

In the next chapter, the investigation into the high speed fibre optic link, which is the communication link between the digitiser and the recorder unit is presented.

CHAPTER 4

FIBRE OPTIC LINK

4.1 Introduction

When Kao and Hockham [1966] first proposed the dielectric-fibre surface waveguide for the guided transmission of energy at optical frequencies, the electrical isolation and immunity from EM interference properties of such waveguides were probably not the outstanding features they had in mind for such a transmission medium. The immediate priority was the justification of communication channels which had typical transmission attenuation of 1000 dB/km, as opposed to conductor coaxial links which had about 20 dB/km.

The advances in optical fibre system technology has created wide ranging applications in instrumentation and measurement due to the inherent advantages of fibre optic links. The diverse fields of applications of optical system range from Bio/Chemical to high

voltage and current sensing as well as providing communication systems with excellent electro-magnetic noise rejection and high insulation performance.

The development work carried out for the design and construction of the FOL for use in the DOCTR system is presented in this chapter.

Work was first carried out on the sub-units of the Fibre Optic Link (FOL) using discrete components and Thick Film fabrication technology. The possibility of the DOCTR system going into production brought about another constraint to the development of the system; to standardise the sub-units used in the FOL. The subsequent availability of commercial optical units similar to those developed during this work resulted in choosing 'industry standard' units for the FOL. Further design changes had to be made when the production of those units ceased.

In this chapter, an outline of a Fibre Optic Link is first presented. This is followed by discussion of the properties and features of optical fibre. Features of different types of optical sources used in the optical transmitter and the design of the driver circuit is then followed. A similar work is also presented on the photo-detector and pre-amplifier circuit of the receiver end of the FOL which is the most critical unit of the FOL. The simulation of the driver and receiver circuits are also presented. The construction and testing proceedures of the optical transmitters and receivers are presented towards the end of this chapter.

4.2 The Fibre-Optic Link

A fibre optic link consists of three subunits; the optical transmitter, the transmission medium and the optical receiver as shown in Fig. 4.1.

The optical transmitter consists of an electronic driver circuit and a light source which converts the electrical signal into an optical signal.

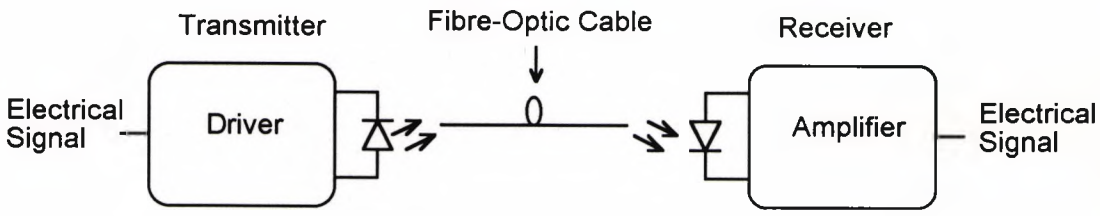


Figure 4.1 Block diagram of Fibre Optic Link

The optical output of the source is launched into the optical fibre cable either directly or through a collimating lens depending on the type of source and cable and application.

The optical receiver consists of a photodetector, which converts the optical signal back into electrical signal, followed by a low-noise amplification stage. Further amplification of the electrical signal may be required before any signal processing is carried out.

The overall performance of such a link is dependent on the characteristics of the individual subcircuits and components which make up the link.

The performance of an optical communication link is characterised by its bandwidth, or the rate at which data is transmitted through the link and the transmitter-receiver spacing or the maximum fibre length before signal distortion causes error in the signal detection.

The overall bandwidth of the link is determined by smallest bandwidth of any component or subcircuit in the link. Therefore the circuit design, layout and technology of the optical driver and receiver must be such that they feature the minimum bandwidth required. In addition the choice of the type of the light source, the photodetector also dictates the performance of the FOL. The fibre optic cable must also be capable of delivering the required bandwidth of the overall system which in turn determine the type of cable suitable for the application. These aspects are discussed in detail in the following sections.

4.3 The Fibre Optic Cable

An optical fibre used for data transmission has a dielectric core through which the light signal is transmitted and this is surrounded by the cladding which has a lower refractive index than that of the core. Light propagates through the core by total internal reflection at the core/cladding interface, made possible by the decrease of the refractive index at the interface.

internal reflection at the core/cladding interface, made possible by the decrease of the refractive index at the interface.

The optical fibres used in optical communications may be classified in three categories depending on their structure and therefore characteristics. They are:

(a) multimode step index

(b) multimode graded index,

(c) single mode step index fibres.

In the following section the characteristics of each type of fibre are cosidered and their performances compared.

4.3.1 Propagation of Waves through the Fibre

A multimode step index fibre has a core of constant refractive index n_1 and a cladding of slightly lower refractive index n_2. Such fibres have large enough diameters to allow the propagation of many modes through the fibre (Fig 4.2(a)).

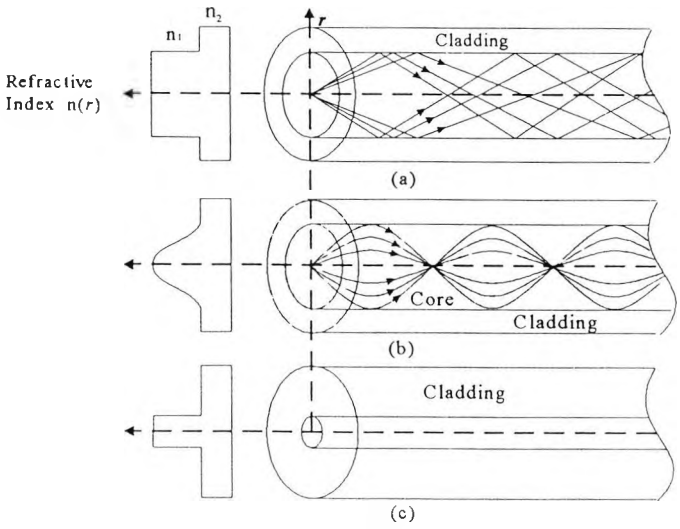


Figure 4.2 Refractive index profile and light propagation through (a) multimode step index (b) multimode graded index and (c) single mode stepindex fibre

These different modes travel at different group velocities and this results in signal dispersion or in the case of digital communication pulse broadening at the receiving end. In addition, the rays which are launched into the fibre at different incidence angles

to the surface of the fibre will have different optical paths through the fibre and therefore the received signal will be distorted. Such fibres are therefore useful in applications where low bandwidth and short lengths of fibre are required. The solution to the difficulties encountered with the multimode step index fibres are either to reduce the fibre diameter such that only one axial ray travels through the fibre or to arrange for the various modes to have a constant travel time through the fibre.

Single mode step index fibres allow the propagation of only one mode and therefore the core diameter is much smaller than that of multimode step index fibres (of the order of 2-10 μm, Fig 4.2(c)). Intermodal dispersion effect or pulse broadening is low in single mode fibres since the delay differences between the various modes are avoided. The bandwidth of the single mode fibre is therefore much higher than that of a multimode step index fibre.

Multimode graded index fibres do not have a constant core refractive index, but a decreasing core index n(r) with radial distance from a maximum value of n_1 at the axis to a constant value n_2 at the cladding (Fig 4.2(b)). Multimode graded index fibres exhibit far less intermodal dispersion than the multimode step index fibres due to their index profile. Although many different modes are excited in the graded index fibre, the different group velocities tend to be normalised by the index grading. Using the ray theory, the rays travelling close to the fibre index have shorter paths compared with the rays which travel into the outer region of the core. However, the near axial rays are transmitted through a region of higher refractive index and therefore travel with a lower velocity ($v = c/n$) than the more extreme rays. This compensates for the shorter path lengths and reduces dispersion in the fibre. It can be shown that graded index fibre exhibits minimum dispersion when they have near parabolic refractive index profile [Senior, 1985]. Such fibres can theoretically have intermodal dispersion performance three orders of magnitude better than multimode step index fibres. Consequently graded index fibres have much higher bandwidths than the multimode step index fibres. Although graded index fibres are not capable of the bandwidths

attainable with single mode fibres, they have the advantage of large core diameters giving greater optical power coupling efficiency between the source and the fibre.

The bandwidth distance product of multimode step index fibre can be up to 25 MHz.km, whereas those of graded index and single mode fibres can be up to 2 GHz.km and 40 GHz.km respectively, [Senior, 1985]. The fibre used for this work is a multimode graded index fibre of 62.5 μm diameter.

4.3.2 Attenuation

Fibre attenuation due to material absorption is a loss mechanism related to the material composition and the fabrication process of the fibre, which results in the dissipation of some of transmitted optical power as heat in the waveguide. The absorption of light may be intrinsic (due to interaction with major components of the glass) or extrinsic (caused by impurities within the glass).

Linear scattering mechanisms cause the transfer of some or all of the optical power contained within one propagating mode to be transferred linearly (i.e. proportional to mode power) into a different mode. This process tends to result in attenuation of the transmitted light as the transfer may be a leaky or radiation mode which does not continue to propagate within the fibre core, but is radiated from the fibre. Two major types of linear scattering are Rayleigh and Mie scattering.

Non-linear scattering causes the optical power from one mode to be transferred in either the forward or backward direction to the same, or other modes. It depends critically upon the optical power density within the fibre. The major types of non-linear scattering are Brillouin and Raman scattering, which are significant at high optical power levels.

Optical fibres suffer radiation losses at bends or curves on their paths. Severe attenuation of the guided modes occur at fibre bends with curvature radius of 1 mm at wavelength of 1.55 μm.

Overall attenuation of silica-rich fibre is at present about 0.2 dB/km in the long wavelength region (Fig. 4.3), further discussion is presented later in the chapter.

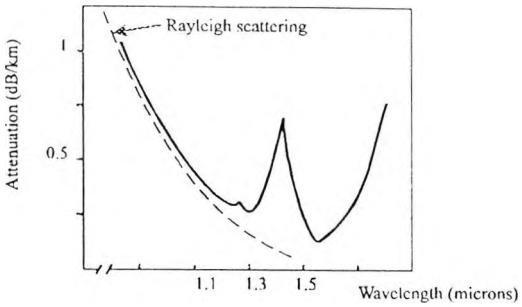


Figure 4.3 Attenuation spectrum of silica-based fibre

4.3.3 Dispersion

Dispersion of the transmitted optical signal causes distortion for both digital and analogue transmission along optical fibres. In digital links, dispersion causes broadening of the transmitted pulses as they travel along the channel. Intersymbol interference (ISI) occurs when the pulse broadens sufficiently to overlap with its neighbours (Fig 4.4) resulting in detection errors at the receiver end.

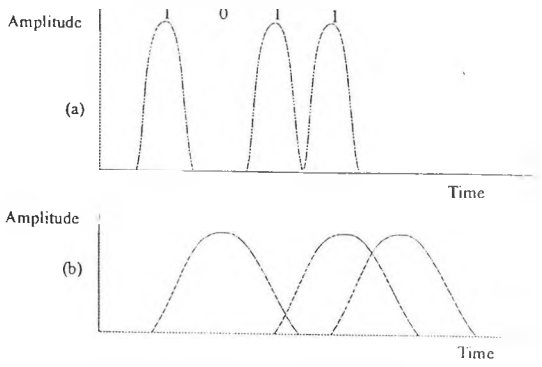


Figure 4.4 Illustration of ISI due to pulse broadening

The error rate is also a function of the signal attenuation of the link. Signal dispersion and fibre attenuation limit the maximum possible bandwidth attainable by a fibre. The dispersion is usually measured by the broadening of a light pulse propagating across the fibre. There are two major dispersive mechanisms which affect the integrity of a pulse (in digital systems); material dispersion and intermodal (or simply modal) dispersion.

Material dispersion may limit the bandwidth of all types of fibre. Material dispersion produces pulse broadening because the light propagation velocity is a function of the wavelength. It has been shown that material dispersion is zero for wavelengths of around 1.27 μm (Fig 4.5), [Payne and Gambling, 1973].

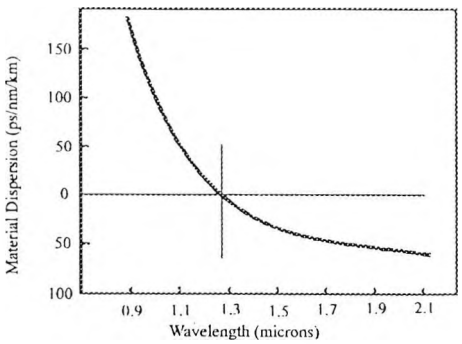


Figure 4.5 Material Dispersion as a function of wavelength for Silica Fibre

Another phenomena which results in pulse broadening is the propagation delay differences of the various modes within a multimode fibre. This is therefore referred to as intermodal dispersion. As the different modes which constitute a pulse in a multimode fibre travel along the channel at different velocities, the pulse width at the output is dependent upon the transmission times of the slowest and the fastest modes. The multimode step index fibre exhibits a large amount of intermodal dispersion which gives the greatest pulse broadening.

Intermodal dispersion is reduced to a minimum in graded index fibres which have parabolic profile. The overall pulse broadening in graded index fibres is far less than that in multimode step index fibres. Single mode fibres exhibit negligible intermodal dispersion and pulse broadening is mainly due to the material dispersion of the fibre.

4.3.4 Modal Noise

Another source of optical signal distortion is modal noise which is caused by the interference between different propagating fibre modes generating a "speckle pattern" across the fibre core which is highly dependent on temperature and wavelength variation of the optical source [Epworth, 1978; Rawson, 1980; Epworth, 1983]. Modal noise is very serious particularly for analogue fibre optic systems. It should be

noted that going to single-mode fibres does not completely solve the modal noise problem. This is because cylindrical single mode fibres actually support two orthogonally polarised modes which propagate at slightly different velocities due to birefringence effects in the fibres (caused by fibre bends, internal stresses etc.). This is known as polarisation modal noise [Epworth, 1981] It can be minimised by using low-birefringent or polarisation maintaining single mode fibres.

4.4 Optical Transmitter

In fibre-optic communication the term optical transmitter is generally given to the light source launching optical signals into an optical fibre in conjunction with the electronic circuitry which drives the light source. The light source effectively converts the electrical signals to optical ones before being transmitted through the fibre. In this section we shall consider the different types of optical sources which are suitable for fibre-optic communication and on the basis of the requirements of the link to be used in the recorder system of this work, a particular optical source is selected. The driver circuit for the optical source is then discussed.

4.4.1 Optical Source

Light sources that are commonly used in fibre optic communications may be classified in two categories depending on the process involved in producing the light output:

1. Sources which emit coherent light output as a result of light amplification by stimulated emission conducted, by carrier injections, within the active layers of structural semiconductor materials. These sources are known as semiconductor laser diodes (LD).

2. Light sources which have incoherent light output due to spontaneous emission without an inherent gain mechanism. These sources are known as light emitting diodes (LED).

Laser diodes enjoy a number of important features which LEDs cannot achieve; these are:

- high optical output
- high modulation bandwidths
- very narrow spectral line width.

Laser diodes can have 1-5 mW of optical power launched into an optical fibre and with their very fast response time are capable of transmission rates in the range of several GHz. The narrow spectral width of the laser diode (Fig 4.6(a)) results in low pulse broadening due to modal dispersion. The use of LDs as the optical source allows long haul wideband telecommunications links to be implemented.

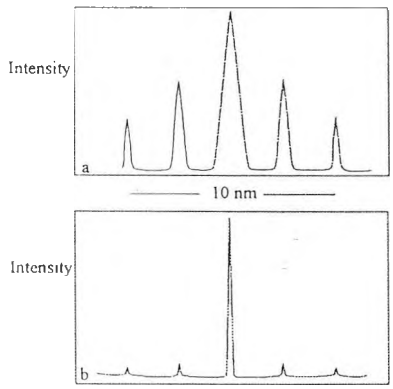


Figure 4.6 LD output spectrum, (a) miltimode laser, (b) single mode laser.

The performance of the optical link is further enhanced when single mode injection lasers are used. Such LDs have spectral width of a few Angstrom units (Fig 4.6(b)) and therefore dispersion is reduced to a minimum allowing longer distances between the transmitter and the receiver. Recent advances in fibre fabrication technology has resulted in enhanced capacity of fibre optic communication systems. One approach has been to shift the minimum dispersion wavelength to 1.55μm where the lowest losses are attained. Such fibres, known as Dispersion Shifted Fibres (DSF), can theoretically attain a transmission rate of 10 GHz for about 500km [El-Refaei, 1987]

One major drawback of the laser diodes is their temperature dependence The LD is a threshold device and the lasing output is proportional to the drive current above the

threshold. The threshold current is not constant but a function of the device temperature and age, (Fig 4.7).

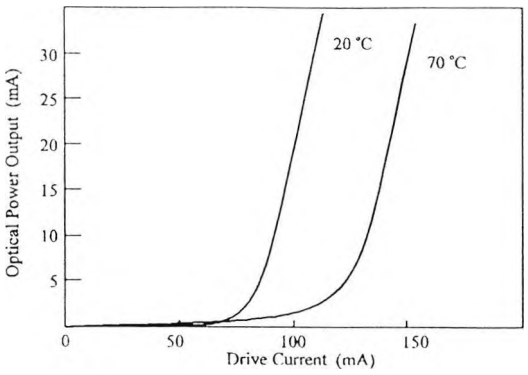


Figure 4.7 LD Output variation with temperature

The threshold currents of typical LDs increase by 1% per degree [Senior, 1985]. Being a threshold device, any significant change in junction temperature may result in considerable change in the operation of the lasing device. This has a significant impact on the drive circuitry. Temperature compensation and feedback techniques are used in the transmitter design to reduce this limitation.

On the other hand LEDs produce lower optical power levels having wider spectral line widths. In an LED link, the maximum optical power which may be coupled into a multimode fibre is of the order of 1 mW [Ettenburg, 1979], with spectral widths (full width at half power(FWHP)) of 50-100 nm, (Fig 4.8). The typical bandwidths of LEDs are a few hundred MHz, although advances in fabrication technology have produced LEDs with bandwidths in the GHz region [Suzuki, 1984]

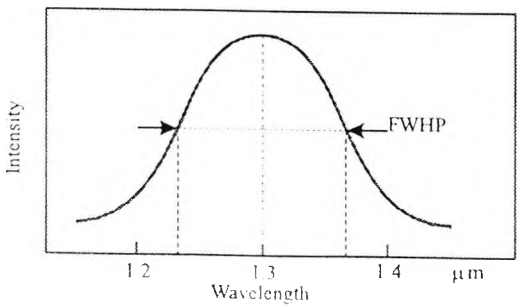


Figure 4.8 LED output spectrum

For applications where bandwidth-distance product of 1000 GHz.km is not required, LEDs have a number of advantages over injection lasers:

- Reliability and longer life cycle,
- Less temperature dependence
- Simpler drive circuitry.

In addition, Laser diodes have a predicted mean time to failure (MTTF) of $10^5 - 10^6$ hours whereas LEDs have an MTTF of 10^9 hours [Kressel, 1982]. The optical output of an LED is also dependent on the device junction temperature, but this does not critically affect the operation of the device due to its lack of threshold. For digital transmitters the almost linear I/O characteristics of the LED (Fig 4.9) contribute to the relative simplicity of the drive circuit required. Analogue transmitters using LEDs as optical source require a more complex drive circuit; this will be referred to later in this chapter.

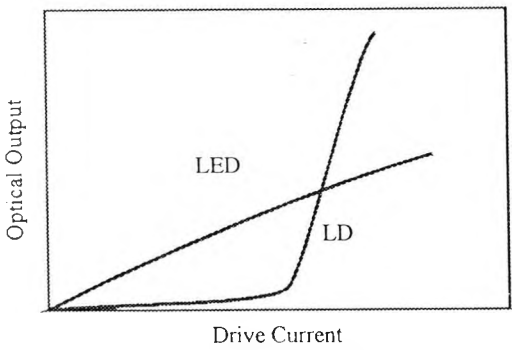


Figure 4.9 I/O Characterstics of LD and LED

For this project the length of the fibre-optic link (FOL) is not required to be more than a few hundred meters. In this recording system, the transmission rate through the link is expected to be not more than a few hundred MHz depending on the maximum sampling rate attained by the ADC or the maximum recording rate achievable for the RAMs in the recorder unit; the slowest determines the overall speed of the system.

From the above discussion it is clear that the use of laser diodes for this work cannot be justified especially as an LED-based transmission system would be more reliable because of the simplicity of the driver circuit and the longer life of optical source.

Having selected the type of optical source to be used in the FOL, we shall consider the different types of LEDs and decide the most suitable one for this application.

4.4.2 Surface and Edge Emitting LEDs

Depending on the structure of the device, LEDs used for fibre optic communication are of two types: surface emitting LEDs, (SLED) and edge emitting LEDs (ELED).

As their names imply, surface emitting LEDs have their larger active region on the surface of the devices structure. Edge emitting devices on the other hand, have their active region sandwiched between the various layers of the structure similar to the geometry of a laser diode, with the light produced being guided by the layers of the structure to the edge of the device. The emitting areas of ELEDs are thus smaller than those of SLEDs [Senior, 1985]. Although both device types exhibit a number of similarities in terms of their general performance, there are significant differences between them in terms of important characteristics such as output power levels, bandwidth, spectral width and coupling efficiency. The overall optical output of a surface emitting diode is higher than that of an edge emitting one, as can be seen from the input/output characteristics of Fig 4.10. However, because the SLEDs have a larger emitting area than ELEDs, their outputs are spread over a greater volume. Therefore it is more meaningful to compare the radiance of the sources than their total output power. The radiance is the optical power emitted from a unit area of a device into a unit solid angle and is expressed in units of $Wcm^{-2}sr^{-1}$.

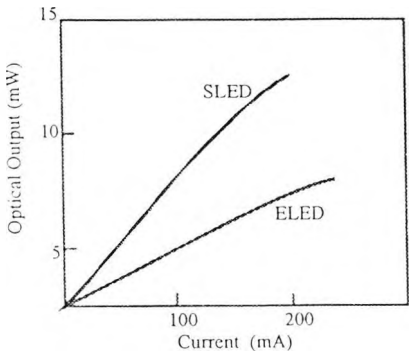


Figure 4.10 Emitted Power Profile of SLED and ELED

Although surface emitters generally radiate more power into the air (around 3 times) for a given current than edge emitters, the waveguide structure of the ELEDs results in a higher effective radiance and this allows better coupling efficiencies with optical fibres. Theoretically, an ELED can couple 7.5 times more power into low numerical aperture (NA) fibre than a comparable SLED, but in practice the increased efficiency obtained is around 6 times [Marcuse, 1977; Botez, 1979]. It is only when a lens is used that the coupling efficiency of an SLED into a fibre becomes comparable to that of an ELED coupling.

Another important difference between the surface and edge emitters is their response capabilities. The SLEDs have bandwidths of around 20 MHz whereas ELEDs have bandwidths of more than 100 MHz [Kressel, 1982; Botez, 1979]. In addition a feature which is significant in high speed longer distance applications is the spectral width of the light input of optical source. As mentioned earlier with wider spectral width of the optical signal, the effect of intermodal dispersion and therefore intersymbol interference is enhanced which in turn reduces the maximum bandwidth distance product attainable. The total light pulse broadening Δt, is given by

$$(\Delta t)^2 = (\Delta t)^2_{spectral\ dispersion} + (\Delta t)^2_{modal\ dispersion}$$

It has been demonstrated that a three fold decrease in the spectral width of the LED output results in a similar increase in the bandwidth of the system [Kressel, 1982]. ELEDs can produce light outputs with spectral line widths of less than 50 nm whereas SLEDs have outputs with spectral widths of around 100 nm [Olsen et al, 1981; Wada et al, 1981]. Therefore ELEDs provide superior performance in terms of bandwidth-distance product to SLED due to the former's higher coupling efficiency, bandwidth and narrow spectral width of the optical output.

The wavelength of the LED output also plays an important role in the bandwidth-distance product performance. As mentioned earlier in Section 4.3, the optical loss or the fibre attenuation is near a minimum at around 1.3 μm (Fig 4.3). The attenuation is

slightly lower at 1.55 μm. Another incentive to operate in the 1.3μm wavelength is that the material dispersion of high-silica fibre is zero in this region (Fig 4.5). Therefore in order to achieve minimum signal distortion and attenuation, an ELED is chosen which operates at 1.3μm wavelength.

Intrinsically the LED is a linear device compared to laser diodes (Fig 4.9). In practice, LEDs exhibit non-linearities which are significant in analogue transmission where the optical source must follow the input signal linearly [Straus, 1979]. To overcome these effects some form of linearising circuit techniques (such as pre-distortion linearisation, or negative feedback) are used [Straus, 1978]. In digital transmission such non-linearities do not effect the integrity of the system since only two distinct levels are transmitted which have relatively large difference between them. Digital transmission therefore is far less sensitive to source non-linearities than analogue transmission.

In summary, a light emitting diode is chosen as the optical source of the FOL for the application of this work as opposed to a laser diode. The features provided by the latter are not required for this application. An edge emitting type of LED is selected because of its superior performance over the surface emitting type. The source is selected to operate in the wavelength region (of 1.3μm) at which the fibre presents near minimum attenuation and zero material dispersion.

4.4.3 Driver Circuit

In this section different LED driver circuits are reviewed, illustrating the build up to the final circuit configuration used for the LED driver for the optical link.

At the start of this work, extensive analytical work was carried out on the various transistor circuit designs for the LED driver, using Hybrid-π transistor model. This analysis helped to assess the behaviour and performance of the circuit in terms of the bandwidth limitation and stability imposed by the passive and the parameters values of the active components used in the design. It is not possible to include the large volume of this analytical work in the limited space available here. Another reason for not

including this was the subsequent availability of the transistor circuit simulation package SPICE. The presentation of the analysis of the LED driver, and the preamplifier circuit of the optical receiver, using the SPICE simulation records is not only very convenient, but allows the use of enhanced transistor models . The role of SPICE is, of course, to take on the computational work of the analysis, but the parameter values of the transistor model, which were not generally available, still had to be achieved independently. At this stage of the development of SPICE the parameter measurement techniques were being actively pursued. This parameter extraction process and the simulation results are discussed following this LED driver review.

A digital LED driver circuit must switch a current, of about 50 mA, ON and OFF at high speed through the LED in response to data input signals.

There are several circuit configurations for the LED driver and they may be grouped into two classes depending on whether they provide the LED with a step current or a step voltage, (i.e. a current source type or a voltage source type).

The simplest form of low-impedance (voltage source type) driver is the emitter follower (common collector) circuit shown in Fig 4.11.

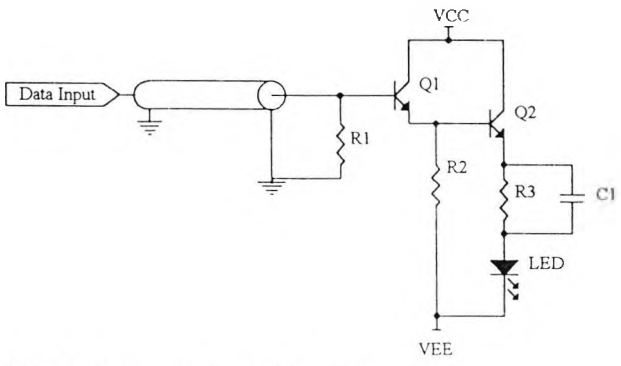


FIG. 4.11 Common collector LED driver

The combination of the two consecutive emitter followers reduces the source impedance seen by the LED and the circuit analysis zero provided by C_1 compensates for the pole arising from R_3 The addition of C_1 enhances the speed performance of

the circuit giving a transmission capability of 100 Mb/s [White, 1973]. R_1 is the matching impedance for the input cable.

Another type of low impedance driver is the current-shunt configuration shown in Fig 4.12.

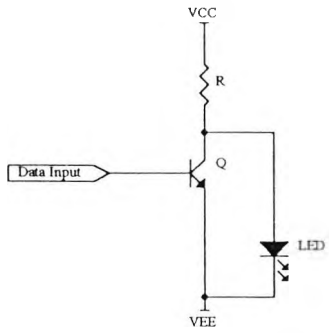


FIG. 4.12 Current shunt LED driver

In this case the switching transistor is placed in parallel with the LED, providing a low impedance path for turning off the LED by shunting current around it. The bandwidth of such optical transmitter is limited by the time constant presented by the collector resistor and diode capacitance. The performance may be enhanced by providing a constant bias for the LED. This may be achieved by a resistor is series with the LED. The pole arising from this resistor may be compensated by a capacitor across it.

In the case of current source type driver, the simplest circuit configuration is the common emitter circuit shown in Fig 4.13.

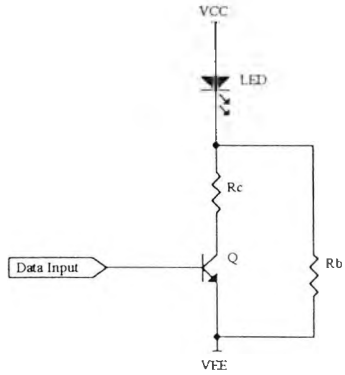


FIG. 4.13 Common emitter type LED driver

In this circuit the transistor switches the collector ON and OFF depending on the input data and in the ON state it presents a constant current and high impedance (of the

reverse-bias collector-base junction) to the LED. Therefore the speed of the circuit will be limited by the input capacitance of the LED. One way to reduce the effect of the LED capacitance is to bias the LED close to the linear region. This bias may be provided by R_b as shown in Fig 4.13. In this way charge is maintained on the LED's capacitance and therefore the drive current is not diverted into charging this capacitance. The speed of the common-emitter switch is limited compared with other configurations discussed earlier. However, when two of these common emitter transistors are put together the important current routing configuration (Fig 4.15) is evolved which offers a performance superior to the other configurations .

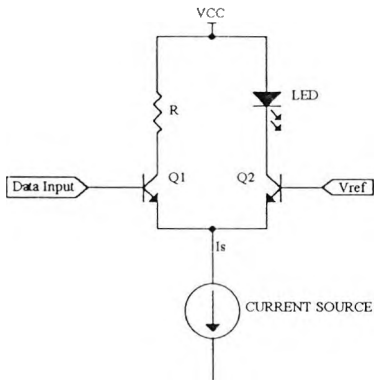


FIG. 4.15 Current-Routing Configuration

It is similar to a differential amplifier [Watson, 1984], but the use of such a circuit as an LED driver is different in two respects from a differential amplifier. First, the collector current of one transistor (of Q_2 in the diagram) is of interest in the LED driver, whereas the difference of the collector voltages of both transistors is required in the differential amplifier. Secondly, the important feature of this configuration as a high speed LED driver is its non-linear characteristic when the circuit is strongly overdriven such that it is operated outside the linear region of operation. It is referred to as a current routing or a current switching configuration [Koelher, 1965]. Fig 4.16 shows the collector currents as a function of the difference of the base voltage. As the base of Q_1 is made more positive with respect to the reference voltage V_{ref}, the current routed to Q_1 increases until Q_2 is cut off. Likewise when the input base is driven strongly negative, Q_1 is cut-off and the current is routed to Q_2.

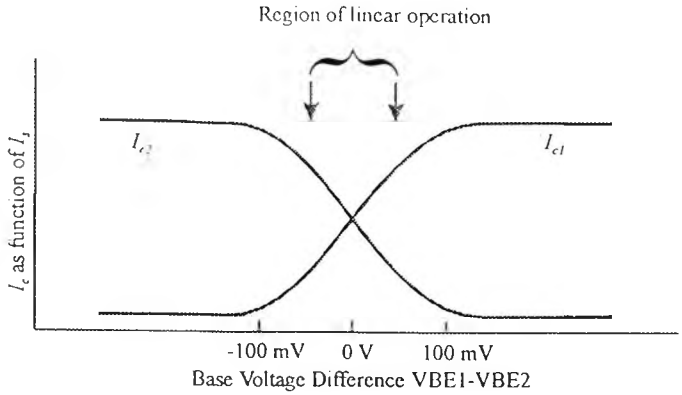


Figure 4.16 Current-routing transfer characteristics

ON/OFF current fluctuation is therefore avoided in this circuit configuration since the constant current is switched from one transistor to another, depending on the input data at the base of Q_1. Fast switching speeds may be obtained due to the non-saturating characteristic of the configuration which avoids switch-off response time degradations caused by stored charge accumulation on the transistor base region. The LED may be loaded to the collector of either transistor ; the output at Q_1 is out-of-phase with the input whereas that at Q_2 is in phase with the input.

For circuit simplicity a resistor may be used to provide the 'constant' current required for the circuit. The performance of the circuit is enhanced if a transistor is used as the constant current source. The current through this transistor is determined by the bias condition and the emitter resistor, Fig 4.17.

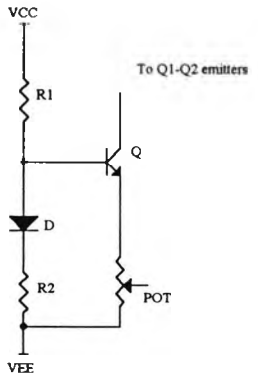


FIG. 4.17 A Transistor Used As A Constant Current Source

A more versatile and yet reliable constant current source is the mirror current source shown in Fig 4.18 [Colclaser et al, 1984]. The current of the mirror source is determined by the programming resistor R_p.

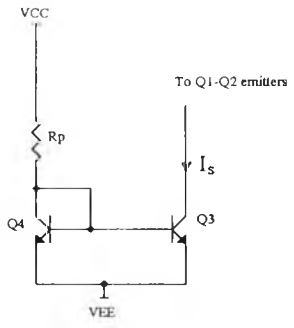


FIG. 4.18 Mirror Current Source

With the collector of Q_4 shorted to its base, the programming current I_p is given by:

$$I_p = \frac{V_{cc} + V_{ee} - V_{BE}}{R_p} \tag{4.1}$$

If Q_3 and Q_4 are identical, then $\beta_3 = \beta_4$ and since Q_3 and Q_4 have the same base-emitter voltage V_{BE}, $I_{B3} = I_{B4}$ and $I_{c3} = I_{c4}$

$$I_p = I_{c4} + I_{B4} + I_{B3} = I_{c4} + \frac{2 I_{c4}}{\beta}$$

$$I_p = I_{c4}(1 + \frac{2}{\beta}) \approx I_{c4} \quad \textit{for typically large } \beta. \tag{4.2}$$

and since $I_{c3} = I_{c4}$, Q_3 mirrors the programming current I_p in Q_4.

In such configurations, because the two transistors are of the same type and they may be fabricated on the same die, difference in temperature variation between the two transistors are avoided, i.e. both transistors, Q_3 and Q_4, have identical V_{BE} temperature variations. I_s is essentially temperature insensitive. The overall LED driver circuit using current-routing and mirror current source configurations is shown in Fig 4.19.

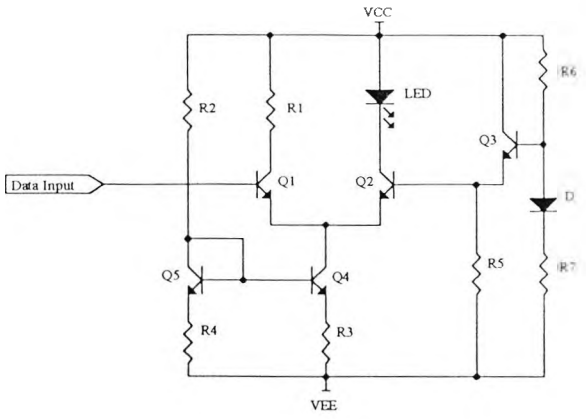


FIG. 4.19 LED DRIVER

4.4.4 Circuit Simulation

The circuit analysis package used for the performance evaluation of the optical driver (and receiver) circuits using discrete components was the Simulation Program with Integrated Circuit Emphasis or SPICE. SPICE was originally developed at the University of California and has since undergone several modifications. The SPICE version used during this work was the 2G5 which had recently become available. SPICE is capable of such tasks as DC, AC and Transient as well as Noise analysis. SPICE has built-in models for semi-conductor devices for which the model parameters have been specified. Four types of semi-conductor devices are used in SPICE 2G5; these are Diodes, Bipolar Junction Transistors (BJTs), Junction Field Effect Transistors (JFETs) and Metal Oxide Semiconductor FETs (MOSFETs). Since BJTs are the transistor types used in this work, only the models for these semiconductor devices are considered here.

The BJT model used in SPICE is based on the integral charge model of Gummel and Poon [1970]. The model reduces to the simpler Ebers-Moll model when certain parameters are not specified in the SPICE program. The Gummel-Poon (GP) model enhances the DC characterisation of the Ebers-Moll (EM) model. In both models, change storage effects, ohmic resistance and current dependent output conductances may be included.

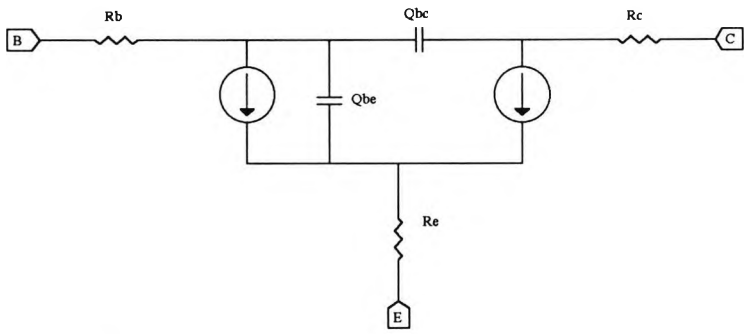


FIG. 4.20 The BJT SPICE Model

The SPICE BJT model is shown in Fig 4.20 [RAL, 1984]. It represents the ohmic resistances which exist between the active regions of the transistor and the external terminals by r_b , r_c , and r_e . The charge storage effects within the device are modelled by the base-emitter (b-e) and the base-collector (b-c) junction capacitances. The base and collector currents are represented by two current generators. Although the model appears simple, it is infact quite a comprehensive one since the interactions between the parameters in Fig 4.20 are also taken into account. There are in fact a total of 40 parameters in the description of the BJT model [RAL, 1984].

4.4.5 Transistor Parameter Extraction

In order to carry out a circuit simulation using, say SPICE, accurate parameter values for the particular device model must be given to the program. For the transistors used, the data provided by the manufacturer was not adequate for the purpose of simulation in two respects. First the data was only provided for a few of the parameters needed and secondly the data was that for the transistor die only and the effects of the packaging of the device had not been determined. Thus it was necessary to evaluate these parameter values before the circuit simulation could begin.

In the following the important parameters which dominate the behaviour of the device and the simplified linear model for a transistor will be briefly considered.

The transistor model parameter extraction process has two different phases; the DC and the Transient (or AC) characterisation phases.

4.4.5.1 DC Characterisation

The DC characteristics of the BJT model are determined by eleven parameters [RAL, 1984], the most important of which are the saturation current I_s, the forward and reverse gain currents β_F and β_R and the Early effect, V_A. Other crucial elements of the transistor model which are determined by the DC characterisation process are the ohmic resistance of the bulk material of the collector and emitter regions to the external terminal of the device. These are represented by r_c and r_e respectively. The resistance between the active base and the base terminal, r_b, is one of the most difficult parameters to measure. The main reason for this is that it is strongly dependent on the operating conditions and is a distributed resistance. It has to be measured under AC condition using the scattering parameter measurement technique.

The forward and reverse current gains are defined by the equations:

$$\beta_F = \frac{I_C}{I_B} \qquad V_{BE} > 0\ ,\ V_{BC} < 0$$
$$\beta_R = \frac{I_E}{I_B} \qquad V_{BE} < 0\ ,\ V_{BC} > 0 \tag{4.3}$$

(i) Acquisition of β_F

The experimental arrangement required to obtain this parameter is shown in Fig 4.21.

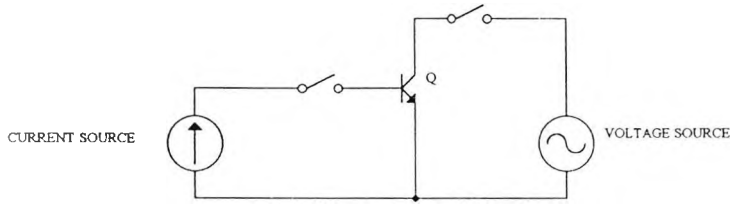


FIG. 4.21 BETA Measurement Arrangement

The current and voltage sources are programmable instruments as are the switches. At operator-defined values of V_{CE}, the current generator is stepped over a user-defined current range and the output current monitored ($\beta_F = \frac{I_c}{I_B}$) Typical results are shown in Fig 4.22.

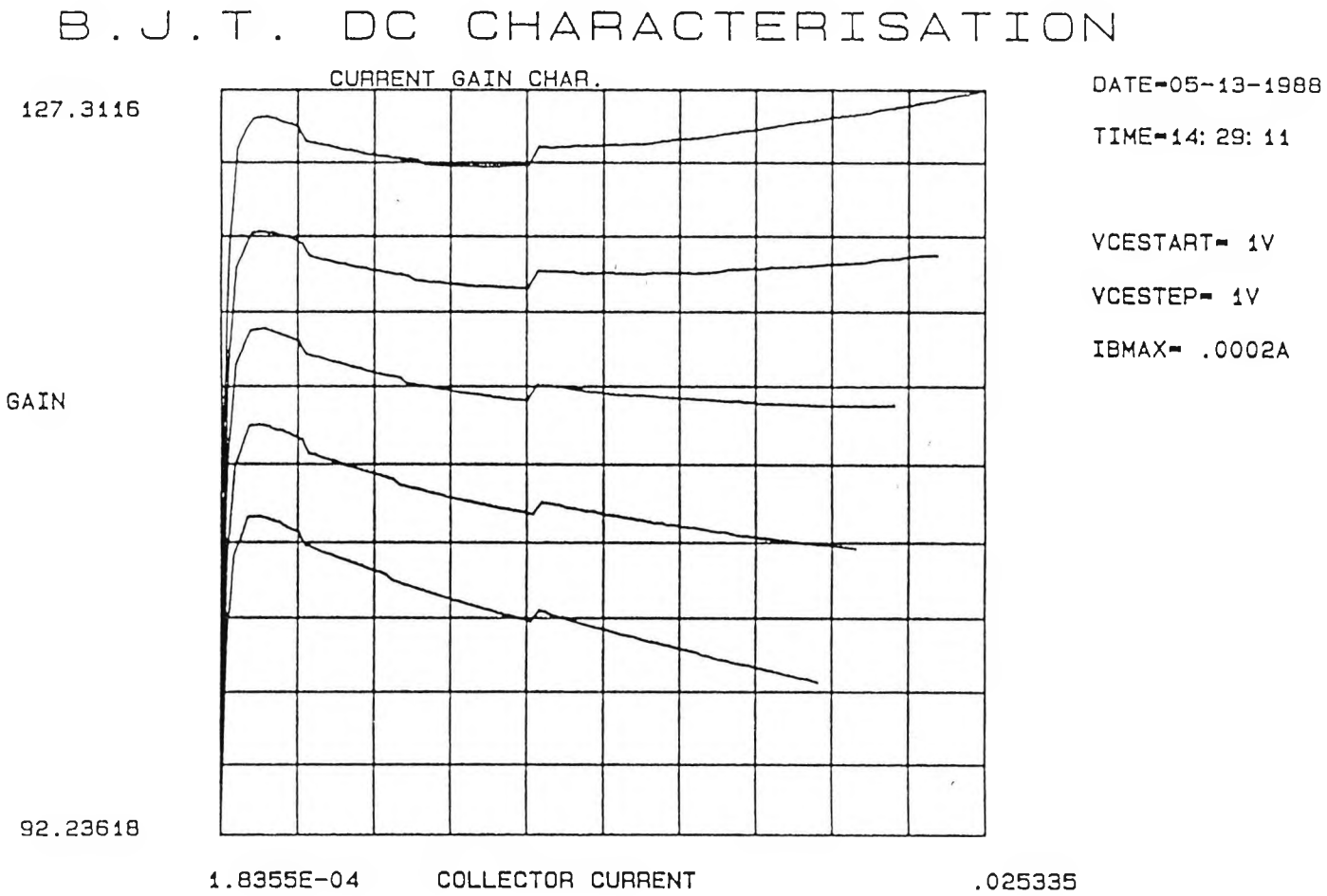


Fig 4.22 Current Gain Charctereristics

It can be seen that the current gain decreases at low values of collector current. There is however a region where the gain remains almost constant.

(ii) Acquisition of β_R

The experiment to obtain this parameter is the same as that for β_F , but the emitter and collector leads must be interchanged so that the reverse current gain is obtained. ($\beta_R = \frac{I_E}{I_B}$)

This parameter shows the same dependence on the current as β_F. The value of β_F and β_R to be used in SPICE are those at the ideal or flat region of the curves. A typical value for this parameter is just under unity. Note that β_F and β_R are dc values and not ac ones.

(iii) Acquisition of I_S (the saturation current)

This parameter is measured with the transistor in the normal active region i.e. forward biased emitter base junction and zero biased base-collector junction. Under these conditions, the collector current is given by:

$$I_C = I_S\{exp(\frac{qV_{BE}}{kT}) - 1\} \qquad (4.4)$$

To make $V_{BC} = 0$ all that is required is to make $V_{BE} = V_{CE}$ and not by shorting the base collector terminals. Typical results are shown in Fig 4.23.

The measurements are performed by injecting a current into the base and adjusting, under computer control, the voltage source until $V_{BE} = V_{CE}$. To obtain the plot shown the measurements are performed at several points.

(iv) r_e

The resistance between the active emitter region and emitter terminal is obtained with the circuit shown in Fig 4.24.

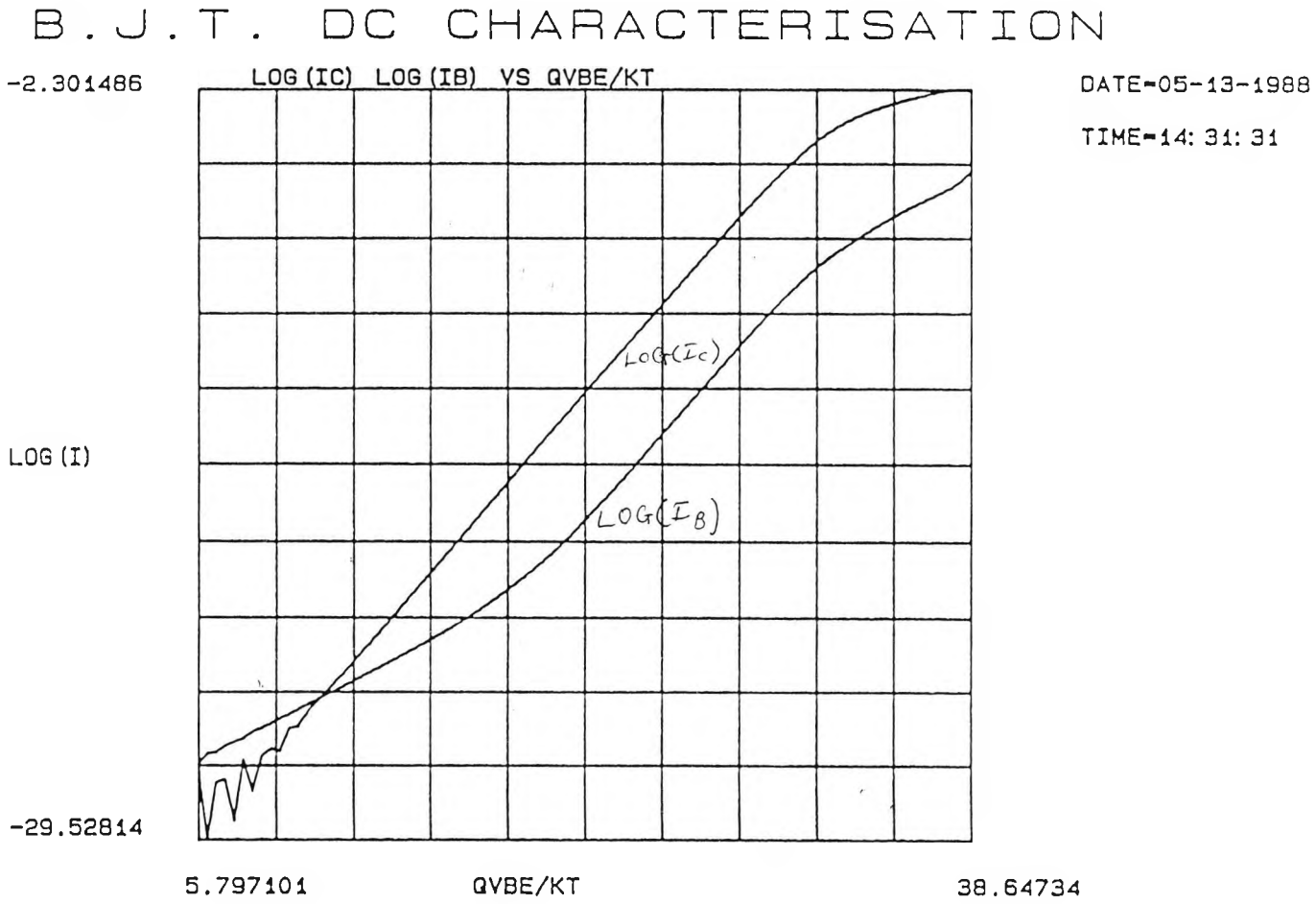


Fig. 4.23 Current vs. VBE.

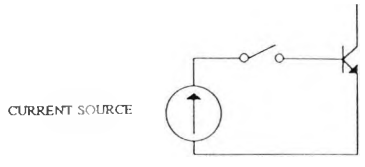


FIG. 4.24 ' re' Measurement Arrangement

With the collector terminal disconnected the programmable current source is stepped over a user-defined current range and the collector-emitter voltage monitored. The resistance between the active collector region and the collector terminal can be simply obtained from the I_C vs. V_{CE} characteristics of the device as shown in Fig 4.25.

Although r_c is assumed to be constant, it actually varies with the operating conditions. The parameter should be evaluated under the same operating conditions as the device will assume in circuit.

As with all the measurements, careful attention must be paid to the stray effects introduced by the jigs and measurement set-ups.

(v) Junction Capacitances

These parameters model the variation of the depletion layer junction capacitances with voltage. With the collector terminal disconnected, the base-emitter is first measured using an LCR (HP-IB controlled) bridge. This measures the capacitance as a function of junction voltage, the voltage range being specified by the user. Similarly the base-collector junction capacitance is measured with the emitter disconnected. It is usual practice to measure the capacitance using a test frequency signal of 1 MHz. Some LCR bridges, however, allow the user to examine the capacitance not only as a function of voltage but also as a function of frequency. Since these parameters model depletion-layer effects, the junction under investigation must be reverse- biased. It is important to realise that before the device is inserted in the jig the measurements set-up must be calibrated to ensure that only the capacitance of the device is measured. Typical graphs for C_{be} and C_{bc} are shown in (Fig. 4.26).

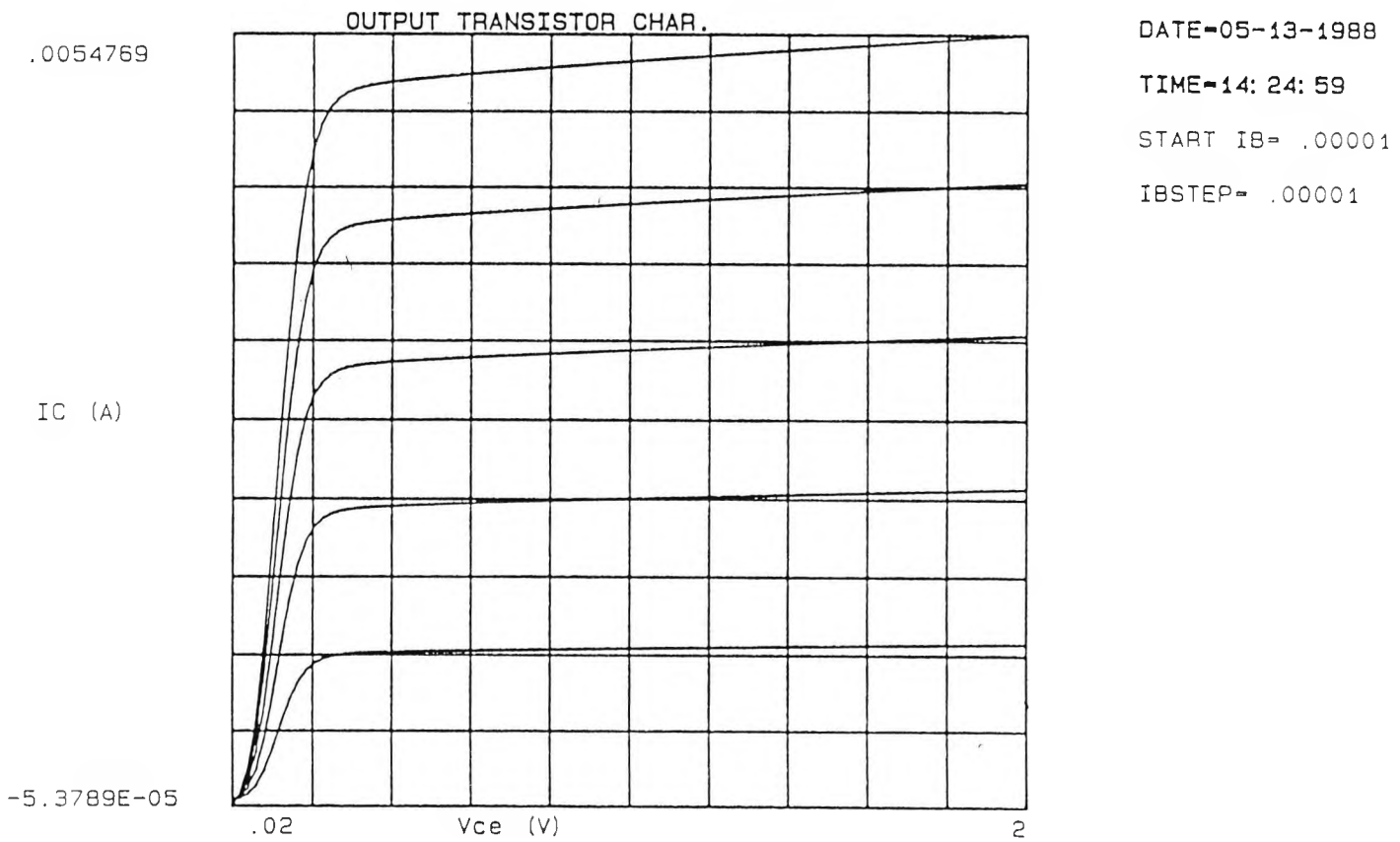


Fig. 4.25 Output Characteristics

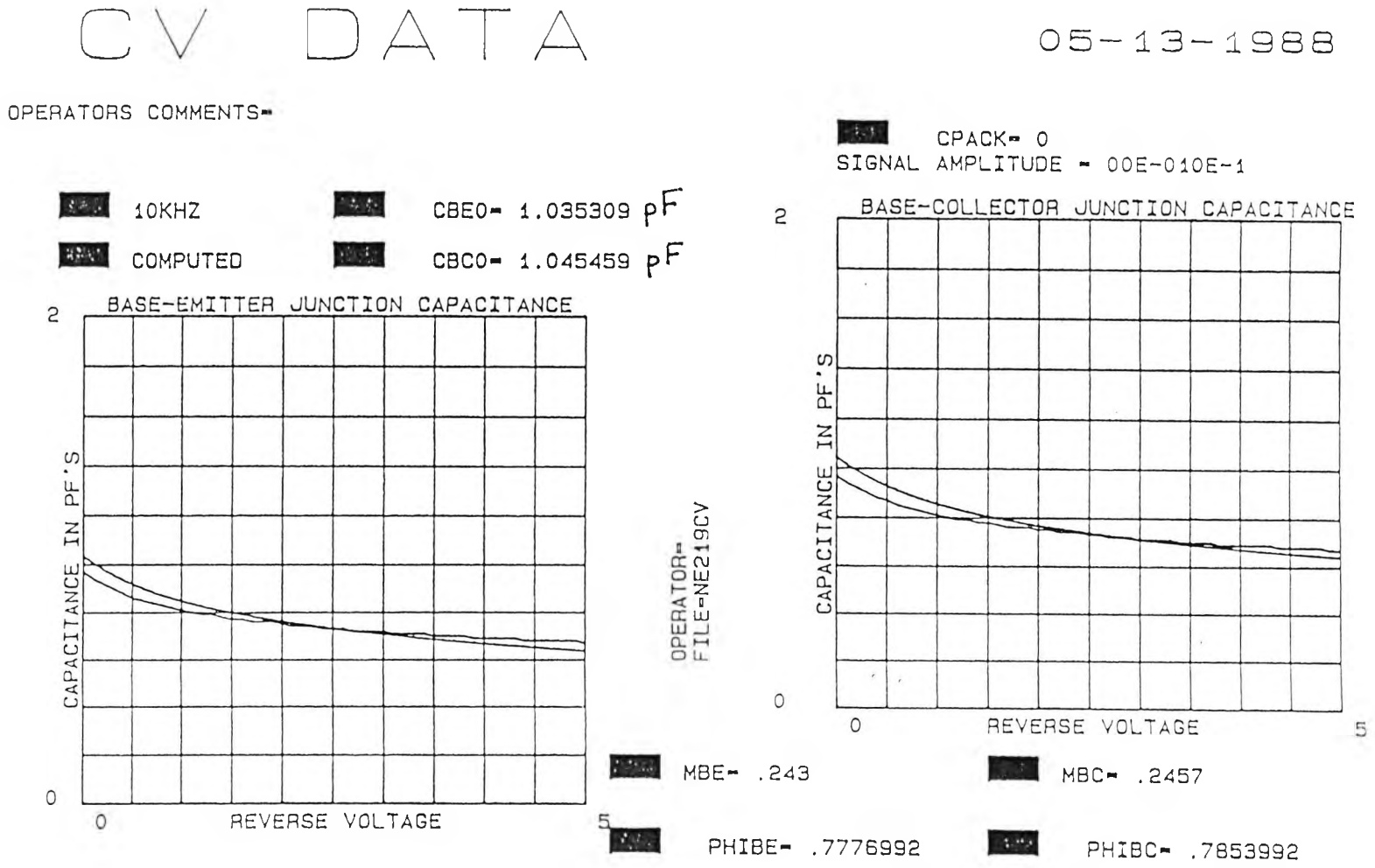


Fig. 4.26 Junction Capacitance Vs voltage

4.4.5.2 AC Characterisation Using S-Parameter Technique

In addition to the base spreading resistance r_b and the charge storage effects at the b-e and b-c junctions of the device, another parameter of the transistor which must be evaluated is the transit time τ, is given by

$$\tau_F = \frac{1}{2\pi f_T} - \frac{kT}{q I_C}\{C_{JE} + C_{JC}(1 + \frac{I_C r_C}{kT/q})\} \qquad (4.5)$$

These parameters must be measured under ac conditions in a transistor model; because of the interactions that exist between the various parameters, measurements of individual parameters in isolation from other effects do not reflect the transistor characteristics accurately. In addition major difficulties are encountered when these parameters are to be measured (using h, y or z-parameter techniques) at high frequencies; the reason being that open or short circuit conditions (required for such techniques) become very difficult to implement.

Scattering parameter, or s-parameter, measurement technique is a relatively simple method which delivers accurate and reliable results for use in transistor characterisation. An important advantage of s-parameters stems from the fact that travelling waves, unlike terminal voltages and currents, do not vary in magnitude at points along a lossless transmission line. This means that scattering parameters can be measured on a device located at some distance from the measurement instrument, provided that the measuring device and the instrument are connected by low-loss transmission lines.

General scattering parameters have been defined by Kurokawa [1965]. These parameters describe the inter-relationship of a new set of variables (a_i, b_i), which are normalised complex voltage waves incident on and reflected from the i^{th} port of a network. The wave functions used to define s-parameters for a two-port network are shown in Fig 4.27. The linear equations describing the two port network in terms of the independent variables a_1, a_2 and the dependent variables b_1, b_2 are given as

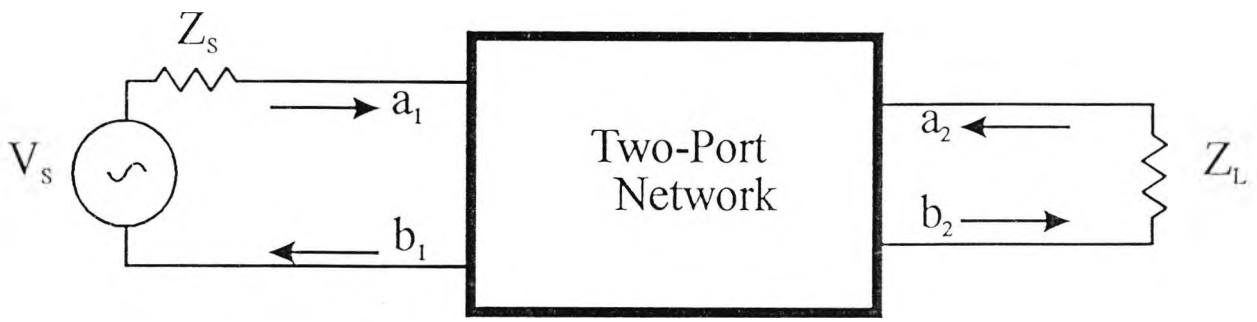


Figure 4.27 Two-port network showing incident (a_1 , a_2) and reflected (b_1 , b_2) waves used in s-parameter definitions.

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2 \qquad (4.6)$$

where the s-parameters s_{11}, s_{12}, s_{21} and s_{22} are

$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0}$ Input reflection coefficient with the output port terminated by a matched load ($Z_L = Z_o$ sets a_2=0)

$s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0}$ Output reflection coefficient with the input matched ($Z_s = Z_o$ and V_s= 0)

$s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$ Forward transmission gain with output port matched

$s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$ Reverse transmission gain with input port matched.

The relationship between the s-parameter set and the other parameter sets (such as h, y, z parameters)are found in relevant literature such as [Hewlett-Packard, 1967].

The parameter values of a transistor model may therefore be evaluated using the s-parameter data.

The s-parameter measurement and the transistor model parameter extraction were carried out by the author at the University of Bradford with the assistance of Dr Rodriguez

The s-parameter measurements were made using an HP network analyser interfaced to a computer to store the measurement data for further processing. Typical outputs of such measurement are shown in Fig 4.28. Each set of s-parameter measurements is carried out under a specific bias condition (e.g. for each value of I_C and/or V_{CE}) for a range of frequencies. Therefore in order to estimate the parameter values of the transistor model over a range of collector currents, say for 10-12 different values of I_C, the s-parameter measurement had to be carried out for each value of I_C.

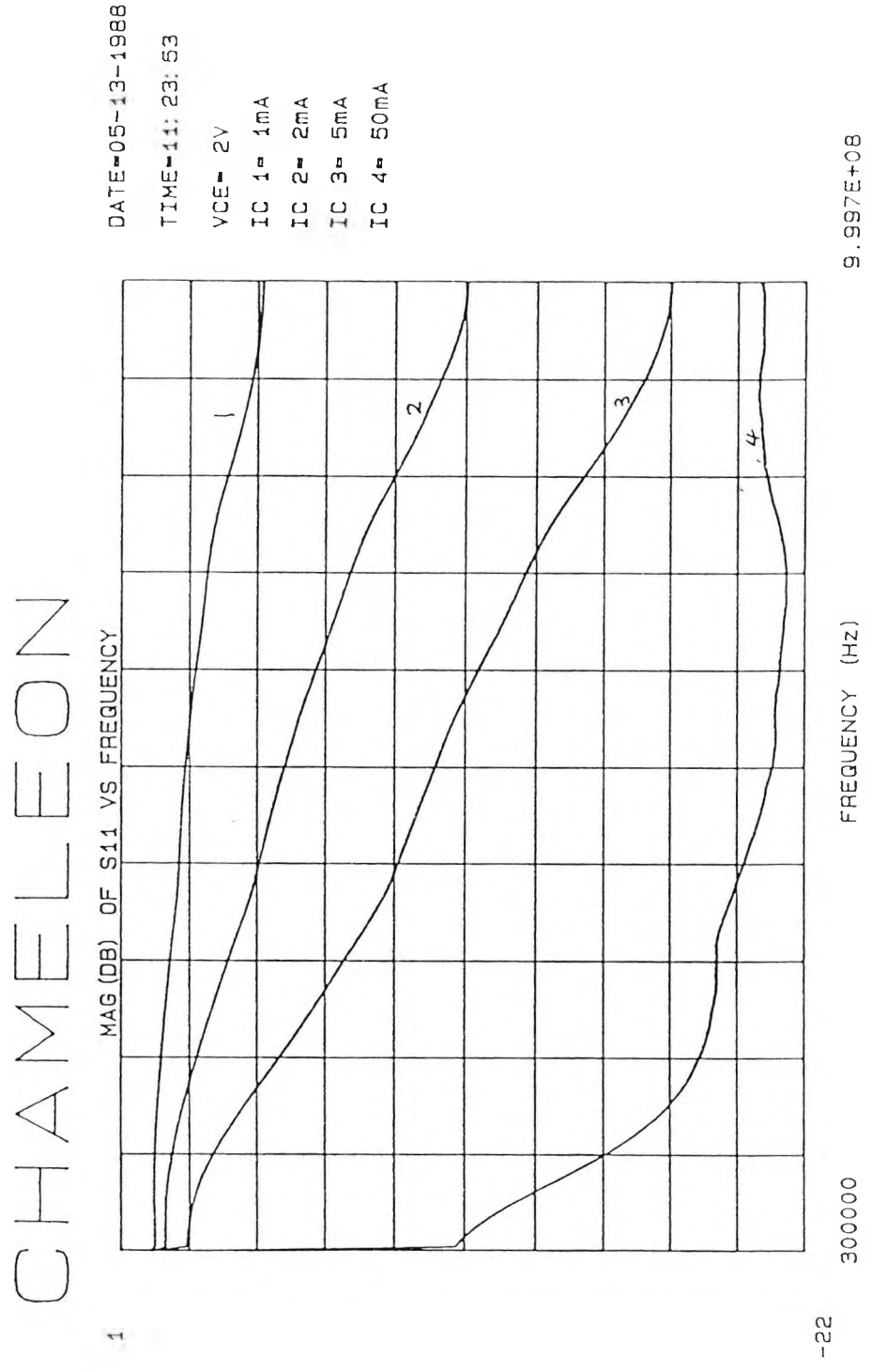


Fig 4.28 (a) s-parameter measurement results: magnitude vs frequency

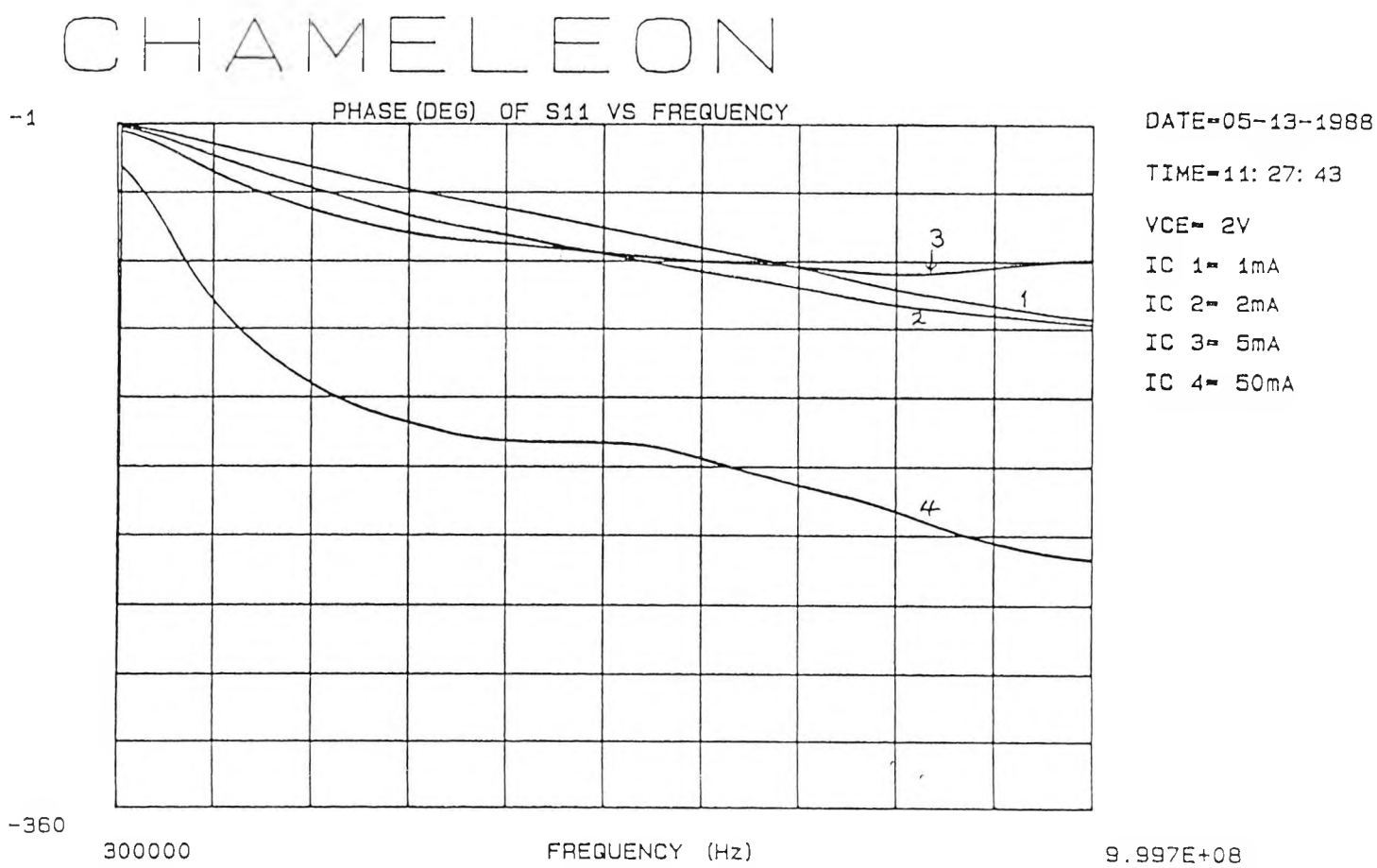


Fig 4.28 (b) s-parameter measurement results phase vs frequency

The model parameter computation process involved an iterative technique to optimise the estimated parameter values for each I_C value (such that the computed values would fit the s-parameter curves).

A significant aspect of this approach for transistor characterisation, from the engineering point of view, is that measurements are carried out taking into account all effects of packaging of the device under test. (The packaging includes the device leads if applicable. Surface mount (SM) transistors were used in this work).

Packaging has crucial effects on the capabilities of the device in high frequencies and must be taken into account in any circuit simulation. The limited data provided by the manufacturers about the device parameter values are usually those of the unpackaged transistor die. It is not appropriate to use such data for circuit simulation when the actual device has a different characteristics due to the packaging effects. Augmented transistor models are proposed and used by engineers to allow for the effects of the device package [Maclean, 1982]. This of course requires the measurement of inductive and capacitive effects of the package itself.

In s-parameter measurement technique, the effects of device package are inherently allowed for. Careful attention must be paid, however, to the jigs used to accommodate the devices. The jigs are therefore calibrated to remove their effects before inserting the device to be measured.

4.4.6 Simulation Results

Transistor-model parameter values obtained from this process were used in the SPICE program and the simulation results for the final driver circuit are shown in Fig 4.29. Fig. 4.29(a) shows the circuit description given to SPICE, and fig. 4.29(b) shows the SPICE output. In this output, the vertical axis is the current driving the LED and the horizontal axis is the time. The current values (of the vertical axis) are printed on the horizontal axis above the printed time values. It can be seen that the collector current (driving the LED) is 48 mA when in the ON state and is about 3.5 mA in the OFF

```
LED DRIVER

****     INPUT LISTING                          TEMPERATURE =    27.0

*********************************************************************

*filename  DRV6_232
VCC 7 0 3.5
VEE 8 0 -5.2
VIN 26 0 PULSE (-1.75 -0.90 0.5NS 0.2NS 0.2NS 2NS 4NS)
RS 26 27 50
T1 27 0 1 0 Z0=50 TD=1NS
R1 0 1 81
R3 1 8 130
Q1 20 1 3 BFQ19
RLED 20 25 14
V1 7 25
Q2 21 4 3 BFQ19
V2 5 21
DLED 7 5 LED
V4 3 22
Q4 22 9 10 BFQ19
R10 10 8 5.6
Q5 9 9 11 BFQ19
R11 11 8 5.6
V5 23 9
R8 23 7 150
Q3 7 6 4 BFQ19/2
R5 4 8 330
R6 7 6 1060
R7 6 12 810
D1 12 13 DIODE
D2 13 8 DIODE
.MODEL BFQ19 NPN IS=7.E-16 BF=50 VJE=0.721 CJE=0.4PF CJC=0.4PF
+ RE=0.5
.MODEL BFQ19/2 NPN IS=7.E-16 BF=50 VJE=0.721 RB=10 RE=2.5
.MODEL LED D RS=4 VJ=1.0
.MODEL DIODE D VJ=0.7
.TRAN 0.1NS 5NS
.PLOT TRAN I(V2)
.PLOT TRAN I(V1)
.END
*****************          ************************  SPICE 2G.5

LED DRIVER
****                    DIODE MODEL PARAMETERS

*********************************************************************

                LED          DIODE
IS          1.00D-14     1.00D-14
RS             4.000        0.000
VJ             1.000        0.700
*****************          ************************  SPICE 2G.5
```

Fig. 4.29(a) Circuit description for the driver circuit.

LED DRIVER
**** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

TIME	I(V2)
0.000D-01	4.754D-02
1.000D-10	4.754D-02
2.000D-10	4.754D-02
3.000D-10	4.754D-02
4.000D-10	4.754D-02
5.000D-10	4.753D-02
6.000D-10	4.754D-02
7.000D-10	4.754D-02
8.000D-10	4.754D-02
9.000D-10	4.754D-02
1.000D-09	4.754D-02
1.100D-09	4.754D-02
1.200D-09	4.754D-02
1.300D-09	4.754D-02
1.400D-09	4.754D-02
1.500D-09	4.755D-02
1.600D-09	4.337D-02
1.700D-09	2.078D-02
1.800D-09	5.230D-03
1.900D-09	3.513D-03
2.000D-09	3.496D-03
2.100D-09	3.483D-03
2.200D-09	3.485D-03
2.300D-09	3.484D-03
2.400D-09	3.484D-03
2.500D-09	3.483D-03
2.600D-09	3.486D-03
2.700D-09	3.484D-03
2.800D-09	3.483D-03
2.900D-09	3.484D-03
3.000D-09	3.485D-03
3.100D-09	3.485D-03
3.200D-09	3.485D-03
3.300D-09	3.484D-03
3.400D-09	3.484D-03
3.500D-09	3.484D-03
3.600D-09	3.484D-03
3.700D-09	3.485D-03
3.800D-09	2.571D-02
3.900D-09	4.984D-02
4.000D-09	4.760D-02
4.100D-09	4.753D-02
4.200D-09	4.754D-02
4.300D-09	4.754D-02
4.400D-09	4.754D-02
4.500D-09	4.753D-02
4.600D-09	4.754D-02
4.700D-09	4.754D-02
4.800D-09	4.754D-02
4.900D-09	4.754D-02
5.000D-09	4.754D-02

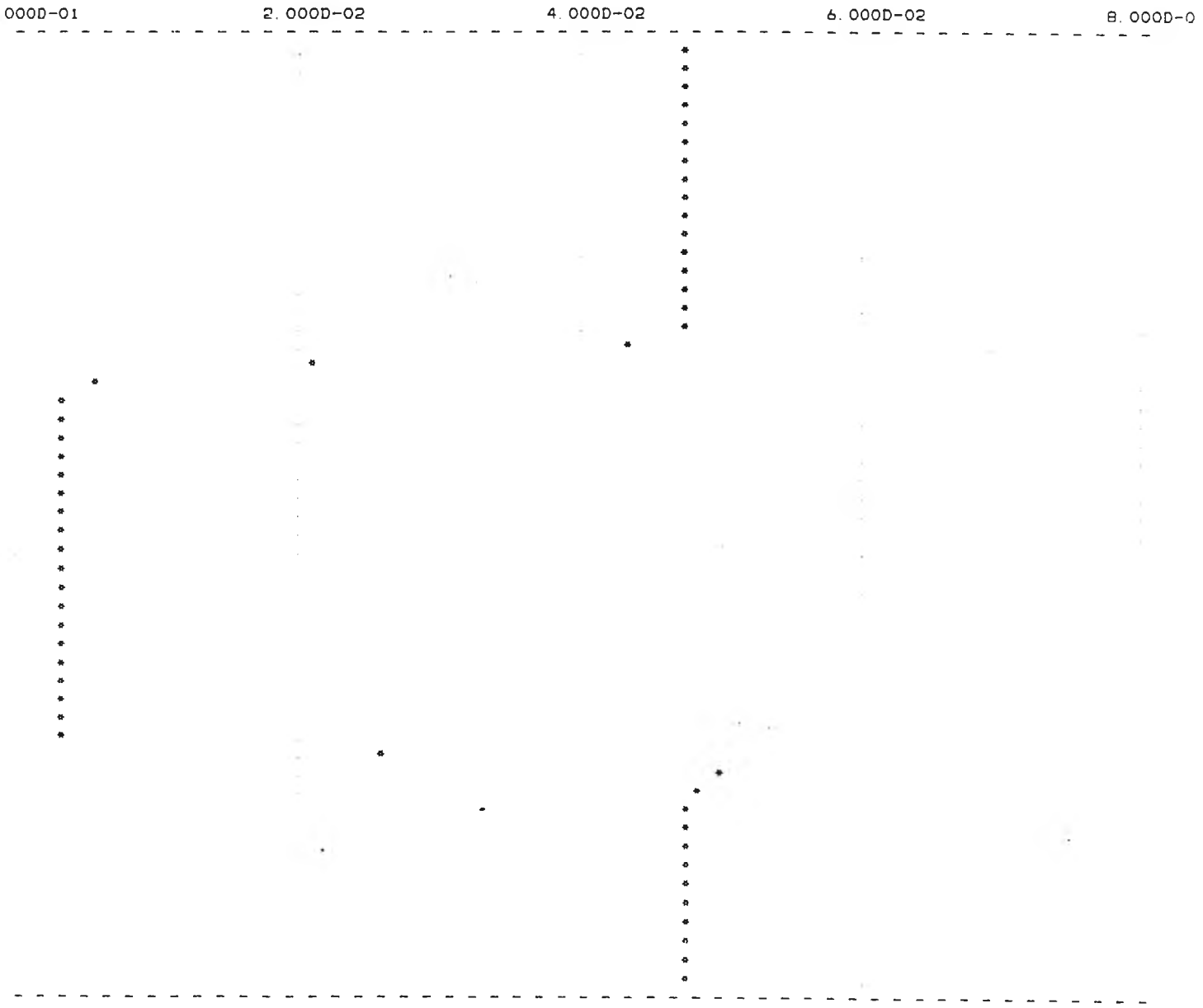


Fig. 4.29(b) Simulation result for the driver circuit

state. The LED is set to be slightly biased in the OFF state to improve its response as mentioned earlier.

4.5 Optical Receiver

The function of the optical receiver is to convert the optical signals received at the end of the optical fibre to electrical ones to be used by the following electronic circuits for subsequent signal amplification and processing. With advances in optical signal processing and optical amplifier design and fabrication technology, optical-to-electrical conversion may not be necessary in future. The objective of the design of the receivers is therefore to achieve this optical-to-electrical conversion with minimum signal distortion. However, there are a number of factors, and also circuit elements of the optical receiver which could contribute to the distortion of the signal during the detection and amplification process. It is important to take into account these factors during the design process in order to reduce their effects and achieve acceptable receiver performance.

The most important receiver characteristics are:

- high receiver sensitivity
- wide dynamic range
- wide bandwidth

Depending on the application, other features of optical receivers may be important, such as bit rate transparency or data format independence.

Receiver sensitivity is defined as the minimum optical power required to achieve the desired Signal-to-Noise Ratio (SNR), for analogue links or Bit-Error Rate (BER), for digital links.

The Dynamic Range is the input optical power range within which the desired receiver operation is achieved (defined by the required SNR/BER, signal integrity and rejection). The Dynamic Range is limited by the minimum detectable optical power which produces the required performance and maximum optical power level before amplifier saturation or overloading occurs resulting in reduced SNR/BER and signal distortion.

The bit rate transparency and the data format independence, as the terms suggest, refer to the receivers' ability to operate satisfactorily without being affected by the bit rate of the incoming data or its transmission code format respectively.

4.5.1 Receiver Components

An optical receiver consists of a photodetector (PD) followed by a low noise amplification stage (pre-amplifier). A post-amplifier is used to boost the signal level for further processing. Following this an equaliser/filter circuit may be needed depending on the receiver specification and circuit design of the preamplifier stage, (Fig. 4.30).

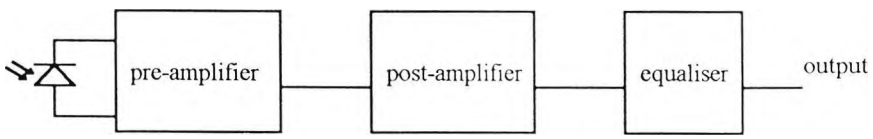


FIG. 4.30 Block Diagram of Optical Receiver

The photodetector, which is reversed biased, collects the optical signal at the end of the optical fibre and produces a photocurrent corresponding to the light signal power incident on its active area.

The preamplifier amplifies the photocurrent and produces the corresponding voltage signal at its output. Because of the low level of the signal involved (the photocurrent) the noise contributions of the preamplifier stage, as well as those of the photodetector itself, have a significant effect on the overall performance of the optical receiver. The circuit design of the preamplifier stage is therefore of utmost importance to the sensitivity of the receiver. The receiver sensitivity is a function of both the photodetector and the following preamplifier. A good preamplifier circuit design could compensate for the noise contribution of the PD. In fact these two components jointly determine the overall performance of the optical receiver.

The post-amplifier provides the signal amplification that is required before further signal processing can be carried out. The post-amplifier may possess features such as

clamping circuits to reference the signal to particular voltage levels or be followed by voltage comparators.

The equaliser is used to compensate for the distortion of the signal due to the combined effects of the pre- and post-amplifiers, or the signal distortion caused by the dispersion effects of the optical fibre.

4.5.2 Photodetector

The most important characteristics of the photodetector (PD) are high responsivity, low dark current and fast response time.

The responsivity (R_o) of a PD is the transfer characteristic of the detector, which is also a measure of the PD's efficiency in converting the optical signal into an electric current. It is defined as the ratio of the output photocurrent (A) to incident optical power(W) $R_o = I_p / P_{opt} \quad AW^{-1}$. Clearly it is desirable to have high PD responsivity as this results in a larger photocurrent and in turn higher sensitivity for the optical receiver. This will reduce the low noise requirements on the preamplifier design. At present, typical values of R_o are around 0.7 A/W.

Dark current is the current generated within the PD with no light incident on the active area of the PD. Dark current is the result of phenomenon such as thermally generated carriers and surface leakage currents. Dark currents have unwanted effects on the receiver performance in terms of noise contribution and therefore need to be as low as possible. The mean square value of the shot noise associated with the dark current of the photodetector may be shown to be [Schink, 1982] $\langle i^2 \rangle = 2qI_D B,$ where B is the effective bandwidth of the receiver. Dark current is also temperature dependent $I_D \propto exp-(\frac{E_g}{kT})$ where E_g is the band energy gap.

The response time (and input capacitance) of the photodetector determine the bandwidth of the device or in the case of a digital system, the maximum bit rate at which the photodetector can operate.

The design requirements for the PD are often conflicting and one feature has to be traded off against another. For instance there is trade-off between the competing effects of fast transit time, requiring narrow depletion region and the low capacitance and high quantum efficiency, η, requiring a wide depletion region. Another example is that dark currents may be minimised by reducing the active area of the device but this undermines the coupling efficiency of light between the optical fibre and the photodetector.

4.5.2.1 Types of Photodetectors

The most commonly used photodetector in fibre optic communication are the positive-intrinsic-negative (PIN) and the avalanche photodiodes (APD). In the following sections these two classes of PD's are considered in more detail with the emphasis on their noise performance.

The **PIN PD** has a simpler structure and is easier to use than APD. The PIN PD has an intrinsic layer sandwiched between the positively and negatively doped regions. The photocurrent at the output of the PIN PD is proportional to the optical power incident on the active region of the photodiode.

In the **APD**, there is a high field region in which the photo-generated carriers (electrons and holes) can acquire sufficient energy to excite new electron-hole pairs leading to avalanche breakdown. This internal current multiplication, which could be as high as 1000, substantially increases the sensitivity of an optical receiver above that of a receiver using PIN photodiodes. On the other hand, the total dark current in an APD is greater than that of a PIN PD. However with the advance in fabrication technology and also by using the III-V compound materials, dark currents may be reduced, e.g. InGaAsP/InP photodiode [Poulin, 1982; Diadiuk, 1981]. By reducing the active area of the photodiode, smaller dark currents are obtained [Mikawa, 1983].

By this means higher sensitivity is achieved, but reduction of the active area of the APD will also reduce the coupling efficiency between the fibre and the APD,

decreasing the optical power collected by the photodiode, which in turn lowers the receiver sensitivity.

Although the APD produces a higher photocurrent than a PIN photodiode there are a number of drawbacks with the APD compared to the PIN photodiode:

- The APD requires high bias voltages (100-400V) to maintain a high electric field.
- The temperature dependence of the avalanche gain necessitates temperature compensation circuits to stabilise the operation of the device. Fig 4.31.

The random nature of the gain mechanism also results in higher noise levels and there are fabrication difficulties associated with the APD structure.

4.5.3 PIN PD Noise Analysis

The noise sources involved in a photodetector fall into two categories: those which depend on the incident optical signal and those which are independent of the signal

The noise source which is independent of the signal level is the dark current associated with each photodetector. The shot noise due to the dark current I_D may be expressed by its mean square value as:

$$\langle i^2 \rangle = 2qI_D B$$

where q is the electronic charge and B is the receiver bandwidth

The signal dependent noise, known as the Quantum Noise, results from the randomness associated with the rate of arrival of the photons at the detector. The photocurrent output of the detector is dictated by the statistical nature of photon arrivals. The number of electron-hole pairs is a random variable with a Poisson distribution characterised by a mean value proportional to the average incident optical power. The photocurrent generated by the photodetector in response to an optical pulse consists of a series of pulses each due to the generation of an electron-hole pair by an absorbed photon. Therefore the photocurrent shot noise as expressed by its

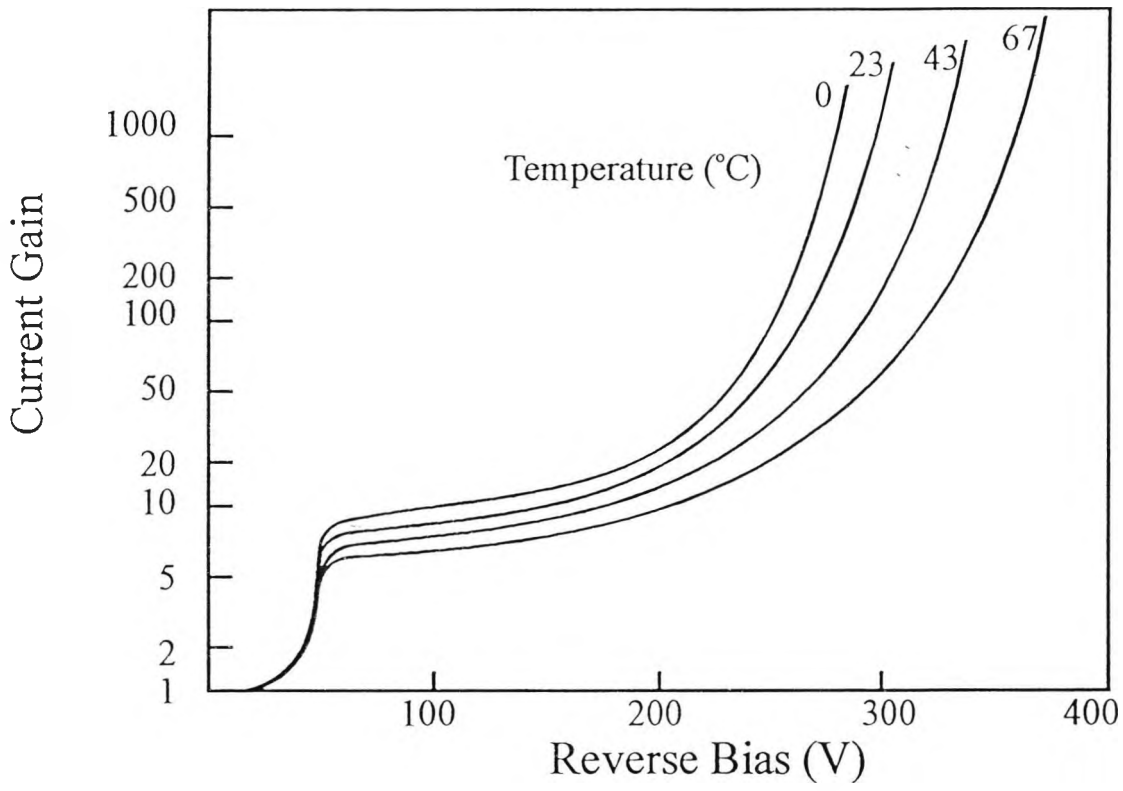


Fig. 4.31 Current gain vs reverse bias for silicon APD

mean square value is given by $\langle i^2 \rangle = 2qI_pB$. The dark current and the quantum noise are the two main sources of noise in PIN PD's and the total shot noise due to these two sources is given by:

$$\langle i_{shot}^2 \rangle = 2q(I_D + I_p)B \tag{4.7}$$

In order to evaluate the SNR for a receiver using a PIN photodetector, the noise contribution of the load resistance and the amplifier must also be considered:

The thermal noise due to the load resistance is given by

$$\langle i_{thermal}^2 \rangle = \frac{4kTB}{R} \tag{4.8}$$

The passive and active elements of the preamplifier following the PD may also contribute to the total noise source of the optical receivers. The amount of this noise, $\langle i_{amplifier}^2 \rangle$, depends on the type of design of the amplifier, details of which are considered in section 4.55.

Therefore the total noise current in an optical receiver using a PIN photodetector is the sum of noise currents due to the dark current, quantum, thermal and amplifier noise. The SNR is therefore the ratio of the photocurrent to the noise current are given by:

$$\frac{S}{N} = \frac{I_p^2}{\langle i_{shot}^2 \rangle + \langle i_{thermal}^2 \rangle + \langle i_{amplifier}^2 \rangle} \tag{4.9}$$

The noise associated with the amplifier $\langle i_{amplifier}^2 \rangle$ may be referred to the load resistor giving the noise figure, F_n for the amplifier [Schwartz, 1970] i.e.

$$\langle i_{thermal}^2 \rangle + \langle i_{amplifier}^2 \rangle = \frac{4kTF_n}{R} \tag{4.10}$$

$$\therefore \frac{S}{N} = \frac{I_p^2}{2q(I_p + I_D)B + \frac{4kTBF_n}{R}} \tag{4.11}$$

4.5.4 APD Noise Analysis

In the case of the APD the nature of the noise sources are more complex than those associated with the PIN diodes for both signal dependent and independent noise source.

The dark current associated with the APD consists of two components one of which is subject to the avalanche multiplication process of the APD or the gain to which the detector is set. The other component is independent of the current gain of the detector. Therefore the dark current for APD may be expressed as

$$I_D = I_1 + GI_2 \qquad (4.12)$$

where I_1 = gain independent component, I_2 = gain dependent component and G = gain.

The signal dependent noise in the APD results from the random nature of the avalanche process as well as the randomness associated with the rate of arrival of the photons at the detector. The latter is a common phenomena for both PIN PD and the APD. For a given gain G, not all of the photogenerated pairs are amplified exactly by G. There is a distribution of gains which is produced by the statistical nature of the avalanche process.

Although the internal gain mechanism increases the output photocurrent of the APD, the dark current and quantum noise are also increased by the avalanche multiplications process and this becomes a limiting factor as far as the receiver sensitivity is concerned. So if the photocurrent is multiplied by a gain factor of G (the mean multiplication factor), then the shot noise is also increased by an excess noise factor G. The total shot noise current of the APD expressed by its mean square value, is given by [Senior, 1985].

$$\langle i^2 \rangle = 2q(I_p + I_D)G^{2+x}B \qquad (4.13)$$

where x = 0.3 - 0.5 for Si and 0.7 - 1 for Ge or III-V APD's

The above equation ignores the effect of the component of the dark current which is not subject to the multiplication process and becomes increasingly insignificant compared to other components in the equation.

Therefore the noise sources of an optical receiver using an APD are the total shot noise current, as given above (eqn. 4.13), and the noise contribution of the load resistor and the amplifier as in eqn. 4.10 since they remain unchanged. The SNR for this case is given by:

$$SNR = \frac{G^2 I_p^2}{2q(I_p + I_D)G^{2+x}B + \frac{4kTBF_n}{R}} \tag{4.14}$$

In the PIN PD case, the dominant noise sources are those due to the thermal and amplifier noise. However in the APD case the shot noise term is the dominant source, since that due to the thermal and amplifier noise is diminished by the avalanche multiplication factor (eqn 4.14). It can be seen that there is a trade off between the high gain for the APD and the high SNR. For low gain values the combined thermal and amplifier term dominates the total noise power and any increases in signal level do not result in a significant increase in the shot noise level therefore increasing the SNR. However for large values of G, the shot noise becomes the significant term and therefore the SNR decreases with increasing G. An optimum value for the gain may be found which corresponds to the maximum SNR given by:

$$G_{optimum}^{2+x} = \frac{4kTF_n}{xq(I_p + I_D)R} \tag{4.15}$$

It can be seen that the optimum gain is dependent on the device and system parameters as well as the operating conditions. The maximum SNR is given by:

$$SNR = \frac{I_p^2}{(2+x)q(I_p + I_D)G^x B} \tag{4.16}$$

4.5.5 Receiver Amplifier Noise Analysis

In the previous section it has been shown that the total noise level in an optical receiver is the result of noise contributions from the photodetector and the front end amplifier and that the noise sources in the photodetector are the photocurrent and dark current shot noises.

The dominant noise sources for an optical receiver are associated with the front end amplifier and the relevant components. The amplifier noise contributions vary depending on the amplifier design and the type of the active device (BJT or FET) used in the design. In the following sections noise analysis for amplifiers employing FET and BJT front ends are presented, taking into account the effects of the high impedance and the trans-impedance design on the receiver noise level.

4.5.5.1 FET Front End Amplifier

The principal sources of noise in this circuit are:

- the noise corner frequency of the FET
- the shot noise associated with the leakage current
- the noise associated with the channel conductance and
- the thermal noise of the equivalent total resistor (of the bias circuit).

The input equivalent amplifier noise is given by [Personick and Smith, 1982]

$$\langle i^2 \rangle = \frac{4kTBI_2}{R} + 2q(I_D + I_{gate})BI_2 + \frac{4kT\Gamma}{g_m}(2\pi C_T)^2\{B^2 f_c I_f + B^3 I_3\} \qquad (4.17)$$

where

B	operating bandwidth
R	load resistor in high impedance design (feedback resistor in transimpedance design)
q	electronic charge
I_{dark}	photodiode dark current
I_{gate}	FET gate leakage current
g_m	FET transconductance
C_T	total input capacitance (including photodiode stray)
f_c	FET noise corner frequency
Γ	FET channel noise factor

k	Boltzmann constant
T	absolute temperature
I_2, I_3, I_f depend	Personick's integrals (normalised noise bandwidth integrals which on received optical pulse shapes and filter characteristics) [Personick, 1973].

The first term in the above equation is the thermal noise due to the load or feedback resistor. This becomes negligible in high impedance designs but is significant in transimpedance designs (due to the relatively low value of the feedback resistor of typically a few $k\Omega$) and could be the dominant source depending on the bit rate.

The second term is associated with photodiode dark current and FET gate leakage current. Clearly it is desirable to have photodiodes and FET with low dark and leakage currents. The third term is due to the FET 's noise corner frequency. The noise corner frequency is defined as the frequency for which the value of the noise is twice the low frequency value [Personick and Smith, 1982]. The fourth term is the contribution from the channel thermal noise.

As mentioned earlier the thermal noise is negligible in high impedance (HZ) designs. The noise contribution from the leakage current and the corner frequency may be minimised by suitable selection of photodiode and FET. The dominant noise source in HZ design using FET front end may therefore be that due to thermal channel noise. In this case the noise contribution varies as B^3 and is proportional to C_T^2.

4.5.5.2 BJT Front End Amplifier

The dominant noise sources in a bipolar transistor are the shot noise due to the base current and the contributions associated with the collector currents and base resistance $r_{bb'}$.

The total input equivalent noise current may be shown to be [Personick and Smith, 1982].

$$\langle i^2 \rangle = 2qI_B BI_2 \qquad \text{base current}$$

$$+\frac{2qI_C}{g_m^2}\left[\left(\frac{1}{R}+\frac{1}{r_{b'e}}\right)^2 BI_2 + (2\pi C_T)^2 B^3 I_3\right] \qquad \text{collector current} \qquad (4.18)$$

$$+4kTr_{b'b}\left[\frac{BI_2}{R^2}+(2\pi)^2(C_d+C_s)^2 B^3 I_3\right] \qquad \text{base resistance}$$

where

I_B & I_C	base and collector currents
g_m	transistor transconductance
$r_{b'e}$	The base-emitter resistance
C_T	The total capacitance including the base emitter and base collector capacitance ($C_T = C_d + C_s + C_{b'e} + C_{b'c}$)
$r_{b'b}$	The base spreading resistance of the transistor
C_d & C_s	The photodiode and parasitic and stray capacitance, with other variables defined in the FET equation

Recalling that $I_B = \frac{I_C}{\beta}$ and $g_m = \frac{qI_C}{kT}$, it can be seen from the noise equation above that the base and collector currents noise contributions are, respectively, directly and inversely proportional to the collector current. Therefore there exists an optimum collector current which minimises the sum of the collector and base current noise contributions. By differentiating the above expression with respect to I_c and neglecting the effect of the changes in $C_{b'e}$ and $C_{b'c}$, the optimum collector current is given by:

$$I_{C_{optimum}} = \frac{kT}{q} 2\pi BC_T \sqrt{\frac{I_3}{I_2}\beta}\left[1+\frac{I_2/I_3}{(2\pi BC_T R)^2}\right]^{\frac{1}{2}} \qquad (4.19)$$

The noise level for the optimum collector current may be obtained by substituting the above expression for I_c in that for the total noise

With the optimum collector current, the circuit noise for a bipolar transistor is given by equation (4.20) below:

$$\langle i^2 \rangle_{minimum} = 8\pi kTB^2 C_T \sqrt{\frac{I_2 I_3}{\beta}}\left[1+\frac{\frac{I_2}{I_3}}{(2\pi BC_T R)^2}\right]^{\frac{1}{2}} + 4kTr_{bb'}\left[(2\pi)^2(C_d+C_s)^2 I_3 B^3 + \frac{BI_2}{R^2}\right]$$

Operating the front end transistor of the amplifier away from the optimum bias current incurs a small noise penalty. Using the above equation for the optimum current, the noise penalty is less than 20% for collector currents of twice the optimum value.

As can be seen from the above equation, the minimum noise for a BJT front end is determined predominantly by a term that increases as B^2 (if $r_{bb'}$ noise is low) whereas the minimum noise for an FET front end is B^3. Consequently an optimally biased BJT input may be superior to an FET input at high data rates.

The $r_{bb'}$ noise contribution is independent of all the circuit parameters except the photodiode and stray capacitance (and of course $r_{bb'}$). Hence $r_{bb'}$ will only add a constant term to $\langle i^2 \rangle$ eqn. (4.18). Unlike the other term in the equation which is proportional to B^2, the $r_{bb'}$ noise component is proportional to B^3 which may become the dominant source of noise in the amplifier at very high frequencies. In order to establish the significance of the base resistance noise to those of the base and collector with respect to the bit rate, the following approach is used. Equating the noise contribution of the base resistance in eqn. (4.18) to those of I_B and I_C gives:

$$r_{b'b}B = 6.5 \times 10^{11} \frac{C_T}{\sqrt{\beta}(C_d + C_s)^2}$$

For $C_T = 6pF$, $(C_d + C_s) = 4pF$ and $\beta = 100$; (4.21)

$$r_{b'b}B = 2.4 \times 10^{10}$$

Thus at B = 300 MHz the effect of the base resistance begins to dominate an optimal bipolar receiver when the front end transistor's $r_{bb'} = 80\ \Omega$.

4.5.5.3 FET versus BJT

The noise for the case FET varies as B^3. In the case of BJT, however, the noise varies as B^2 when $r_{bb'}$ is small and as B^3 when the base resistance noise dominates. Hence at low bit rates the FET is superior whereas at higher bit rates the BJT produces superior performance. The cross over frequency for which the performances are equal is given by equating the noise expressions for each device. Depending on the specific

parameter values the cross over occurs at around 90 MBit/s. [Personick and Smith, 1982]

We had set out for a wideband optical link (300 MHz) and therefore the preamplifier design was based on the BJT front-end which presented better noise performance at the high bit rate.

4.5.6 Preamplifier Design Consideration

The function of the preamplifier is to enhance the very low level photocurrent signal at the output of the preceding photodetector.

There are a number of important characteristics which the amplifier must have to provide the required performance for the optical receiver (i.e. high SNR for analogue system or) low BER (10^{-9} or better depending application) for digital systems. The most important of these are high sensitivity (resulting from low noise contribution from both the photodetector and the preamplifier), wide dynamic range and bandwidth.

These characteristics pose conflicting requirements on the receiver and some might have to be traded off for others in any particular application.

The noise performance of the amplifier is one of the most important characteristics which could affect the receiver sensitivity. Receiver sensitivity is a measure of the minimum optical power required to detect the signal with a given BER fidelity criterion. Although minimum noise performance, or high sensitivity, is the goal in the receiver design, other required features may have conflicting effects on its performance resulting in high noise or less sensitive performance. A wide dynamic range or wide bandwidth are achieved at the cost of lower sensitivity. In contrast to the minimum power requirement, there is a limit to the maximum signal level the amplifier can handle before it is saturated or overloaded. The range between the minimum detectable signal level and the maximum level before the amplifier is saturated is

known as the dynamic range. Dynamic range is another important characteristic of the preamplifier used in the optical receiver.

4.5.7 Amplifier Configurations

Depending on their configurations the front end amplifiers used in optical receivers fall into two categories; high impedance and transimpedance designs.

There are distinct differences between the two design types and each has its own advantages and disadvantages. The operation and relative performance of these designs are discussed in the following sections.

4.5.7.1 High Impedance Design

As suggested by its name, the input impedance of this type of amplifier is high (of the order of MΩ) and therefore the thermal noise contribution due to the amplification stage is very low. Hence in optical receivers employing high impedance amplifiers the noise contribution due to the photodetector (quantum and dark current noise) could be the dominant sources. However, because of the high impedance of this design, the frequency response is limited by the large RC time constant at the input of the amplifier. When the input resistance is large the input admittance is dominated by the input capacitance and the input signal, the photocurrent, tends to be integrated by this capacitance. Thus, the high impedance front end is also known as the integrating front end design.

The signal distortion resulted from the integrating effect of the amplifier is usually compensated for by differentiating the signal using an equalising circuit. This is commonly done after further amplification i.e. at high signal level so that the noise contribution from the equaliser is not significant.

An equalised high impedance amplifier therefore offers the lowest noise level and while retaining the signal integrity. However it suffers from several drawbacks.

The first problem is that the circuit analysis zero of the equaliser circuit has to be matched to the pole position of the amplifier. The amplifier pole position is determined by the values of C_T and R_{in} of the amplifier. The value of the total capacitance C_T includes the stray capacitances and those of the input transistors. The pole position therefore could vary and the matching could be difficult to achieve in production. Also since the amplifier pole can change over the operating lifetime (due to changes in the device parameters) and any resulting pole-zero mismatch could degrade the receiver sensitivity. Adaptive pole-zero cancellation may be used but this further increases the circuit complexity.

Another significant drawback of the high impedance design is its reduced dynamic range which is inherent in the design. Build up of charge on the input capacitance causes premature amplifier saturation. The reduction of dynamic range depends on the amount of integration at the input of the amplifier and the subsequent equalisation. As a general rule the dynamic range is reduced with increasing amount of equalisation.

4.5.7.2 Transimpedance Design

In the transimpedance design negative feedback is used via the shunt resistor R, giving this design several important features.

In such design the feedback stabilises the output voltage response to a current excitation. In addition the use of feedback results in increased bandwidth and dynamic range and decreases the output signal distortion. Furthermore, dependence on transistor parameters is reduced in transimpedance amplifiers and the input and output impedance values may be controlled by the amount of feedback. There is also a direct relationship between the amount of feedback and the bandwidth and dynamic range of the transimpedance amplifier[Maclean, 1982].

A transimpedance amplifier (TZA) is an attractive choice for optical receivers because of the inherent features it possesses which are superior to those of a high impedance

design. The nature of the transfer function of the TZA ($\frac{v_{out}}{i_{in}}$) and its wide bandwidth means that the input signal (i.e. the photocurrent) is not subject to integration or distortion and therefore no equalisation is necessary.

The noise performance of the amplifier is also improved [Maclean, 1982], but the dominant noise source in transimpedance amplifiers is the thermal noise contribution due to the feedback resistor (which is much smaller than that of the input impedance of HZ design). As a result the total noise level of the TZ design is therefore higher than that of the HZ design making the latter to have a higher sensitivity than the former. However optimised TZ amplifiers [Personick and Smith, 1982] have been shown to give a noise performance closely approaching that of a high impedance type. [Hullet and Moustakas, 1981].

In principle the noise level of the TZ design may be reduced by making R_f as large as possible. This has the effect of reducing the bandwidth and the dynamic range of the amplifier. On the other hand, for a desired bandwidth and sensitivity, the open loop gain of the amplifier may be increased, but the maximum open loop gain is ultimately limited by the propagation delay and phase shift of the amplifying stages within the feedback loop. Therefore there is a trade off between high sensitivity and high bandwidth.

4.5.8 Choice of Photodetector and Preamplifier for Receiver

For this application the PIN photodiode (PD) is used in preference to the avalanche photodiode (APD). The PIN PD produces a smaller dark current than the APD and it is constant and has no dependence on the bit rate and it exhibits no great fluctuations with temperature variation. More importantly the PIN diode circuit is much simpler to implement and does not require a high voltage reverse bias. Although higher photocurrents are generated by the APD's due to the avalanche multiplication process, the dark current in the APD also undergoes such a multiplication process and this in

turn reduces the sensitivity of the APD. The overall sensitivity of the APD is still higher than that of the PIN diode.

The circuit required for the APD is more complex than that for PIN diode as a control circuit is required to stabilise the gain of the APD and set it to the optimum value required; too high a gain results in sensitivity degradation of an APD. Also, as indicated earlier, temperature compensation is required as APD gain fluctuations due to temperature variations are significant. The bias voltage required for the APD is between 100-400V [Senior, 1985] as opposed to the nominal reverse bias voltage of around 5V for PIN diode.

Although the high impedance amplifier (HZA) has a superior noise performance and therefore a higher detection sensitivity, it suffers from a number of significant drawbacks such as narrow bandwidth, limited dynamic range and a requirement for equalising circuits to compensate for signal distortion due to the integrating effect at the input of the HZA.

The trans-impedance amplifier (TZA) was chosen since it provides better overall performance than the HZA. The TZA offers superior dynamic range performance and wide bandwidth characteristics. In addition no equalising circuits are required at the output of the TZA. Also in this case the dynamic range is virtually independent of the bit rate at which the amplifier is operating whereas the (smaller) dynamic range of the HZA varies as the bit rate which is not desirable. These bit rate variations are shown in Fig 4.32 [Moui, 1984]. However the TZA exhibits higher noise levels than the HZA because of the dominant thermal noise contribution of the feedback resistor. It can be shown then, in practice, the noise associated with the signal is negligible compared to the circuit noise.

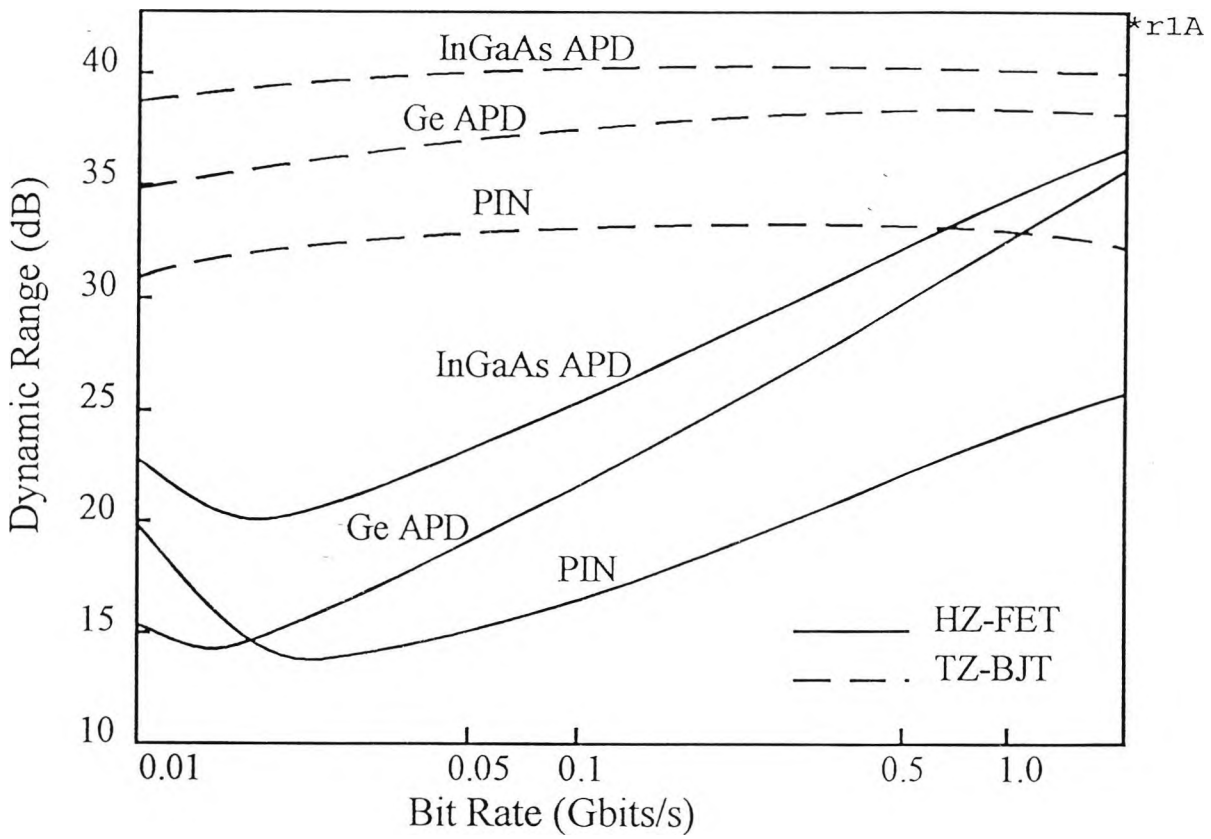


Figure 4.32 Bit range dependence of dynamic range for HZ and TZ designs

4.5.8.1 The Transimpedance Amplifier

The transimpedance amplifier (TZA) is the most commonly used preamplifier design in optical receivers. It is basically a current-to-voltage converter as shown schematically in Fig 4.33

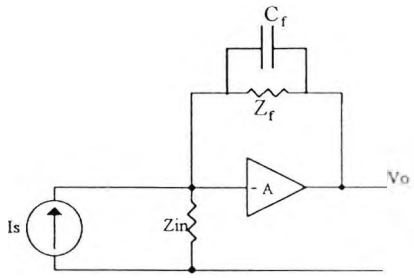


FIG. 4.33 Schematic Diagram of Transimpedance Configuration

It has a transfer function, a trans-impedance, given by:

$$Z_T = \frac{V_o}{I_s} = \frac{Z_o}{1 - \frac{Z_o}{Z_f}} \qquad (4.22)$$

$$Z_o = -A\left(Z_{in} \| Z_f\right)$$

where A = open loop gain of the amplifier

Z_{in} = total input impedance of the amplifier

Z_f = feedback impedance

In practice, however the amplifier gain is finite at high frequencies.The transfer function may contain two or more poles depending on the characteristics of the gain A and the input impedance Z_{in}, which are determined by the details of the circuit design and the values of the components used in the design.

The feedback element Z_f usually consists of a resistor R_f, shunted by its stray capacitance C_f. As far as R_f is concerned, there are conflicting demands on its value. R_f is the dominant noise source and therefore to reduce its level of noise contribution, it must have high values, but on the other hand large values of R_f tend to destabilise it. Another effect of large values of R_f is to reduce the bandwidth of the amplifier.

The response of the amplifier is limited by the time constant CR, where C and R are the input capacitance and resistance respectively. The bandwidth may be increased by reducing C or R or both. Reduction in the value of R is not desirable since this will increase the noise contribution. Therefore only C must be reduced. One way of reducing the capacitance is to use a common-base (CB) transistor configuration between the CE stage and R. This has the effect of reducing the Miller effect [Millman and Hilkias, 1972]. This is because the CB transistor presents a low input impedance. This circuit configuration, CE followed by CB, is known as the cascode configuration (Fig 4.34).

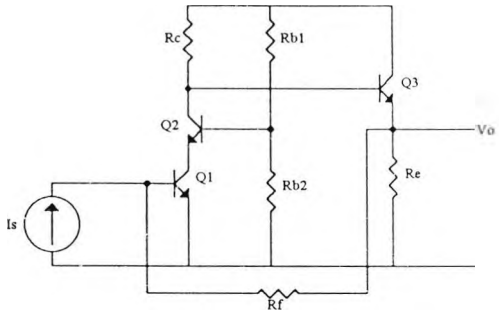


FIG. 4.34 Cascode Configuration (CE-CB)

In addition, the cascode circuit has the very important feature for optical receivers of reduced noise performance compared with the simple CE circuit [El-Diwany, 1981].

As shown in Section 4.5.5.2, the input equivalent noise contribution of the collector current, which also shows prominence when the BJT is optimally biased, is dependent on C_T (eqn. 4.20), the total input capacitance, which is dominated by the b-e and b-c junction capacitance. As the effect of the b-c capacitance is reduced in the cascode design, this in turn results in the reduction of the noise contribution. In cases when the $r_{b'b}$ is small, then the second term in the above equation, becomes negligible and the minimum noise contribution will, for a given current gain β and the required bandwidth, vary as C_T.

Having reduced the effect of $C_{b'c}$, the dominant term in the total capacitance C_T is that of the base-emitter junction of the CE stages i.e. $C_{b'e}$. The effect of $C_{b'e}$ is reduced if an

emitter follower (or common collector, CC) stage is included as the front end of the preamplifier as shown in Fig 4.35

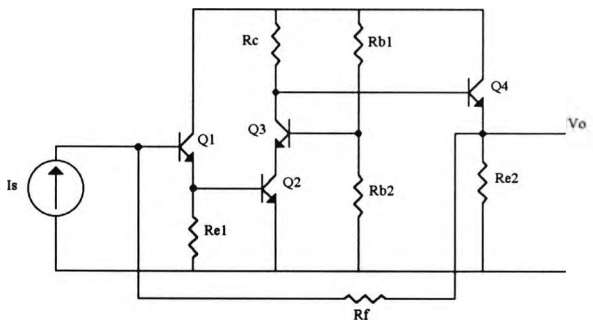


FIG. 4.35 CC-Cascode Configuration

The low output resistance presented by the CC stage reduces the resulting time constant (with $C_{b'e}$) at the input of the CE stage [Sibley, 1982]

$$\tau = R_{OCC}(C_{b'e2} + 2C_{b'c2})$$

$$\text{where} \quad R_{OCC} = \left[\left(\frac{R_f + r_{b'e1} + r_{bb'1}}{h_{fe1}} \| R_e\right) + r_{bb'2}\right] \| r_{b'e2} \tag{4.23}$$

4.5.8.2. Shunt- and Series-Feedback Pairs

Another circuit design philosophy which was investigated during this work (but not implemented) was the combined shunt and series feedback pairs. The idea is to use alternate series and shunt stages to obtain high gain without undermining the stability of the circuit [Cherry and Hooper, 1963]. The draw-back of such design is that the number of stages used in the circuit will limit the bandwidth of the circuit.

In the transimpedance amplifier, the shunt resistor is the dominant noise source of the circuit. In order to reduce this effect, the value of R_f must be made as large as possible. However too large a value results in amplifier instability.

A circuit advantage of the shunt feedback configuration follows from the use of localised feedback which provides for greater open loop stability in the overall amplifier [Cherry and Hooper, 1968]. The choice of a shunt feedback second stage necessitates the use of a third stage within the overall feedback loop, which in itself

serves to increase the gain further. The requirement for the extra stage (series feedback) following the shunt feedback stage is on the basis of the approach suggested by [Cherry and Hooper, 1963] in which alternate stages (shunt-series-feedback) are employed in cascade in order to introduce impedance mismatch between adjacent stages so that there is no substantial interaction. Therefore each stage operates under the condition for which its transfer function was defined and the overall function may be calculated by simply multiplying the individual stage transfer functions. The delay associated with each stage eventually limits the number of stages that can be had for a given bandwidth.

4.5.9 SPICE Simulation of Receiver Circuit

As with the transistors for the driver circuit, a series of s-parameter measurements were carried out at the University of Bradford on a batch of transistors (BFT25) to be used for the receiver circuit. The data from these measurements were used to compute and optimise the parameter values for a linear Hybrid-π model. A linear Hybrid-π transistor model is a simpler version of the Ebers-Moll model and is used to reduce the time taken to arrive at the optimised parameter values of this model. The linear transistor model can be used because the input signal (the photocurrent) to the receiver circuit is very small and the transistor is operated only in the linear region

The parameter values estimated for the linear Hybrid-π transistor model for the BFT25 transistors were used in the SPICE simulation of the receiver circuit. The circuit description of the receiver is shown in Fig 4.36(a). The output of the simulation for AC analysis is given in Fig 4.36(b). Two graphs are shown in Fig 4.36(b); the amplitude and the phase. The amplitude is indicated by '*' and the phase is indicated by '+'. The amplitude and phase axes are shown on the vertical axis and the frequency axis is shown on the horizontal axis. Fig 4.36(b) shows the bandwidth of the circuit to be more than 320 MHz. Fig 4 36(c) shows the SPICE output for transient analysis. It shows a response time of about 1.2 ns. (In SPICE, transient analysis are referred to

```
******* ********  SPICE 2G.5 (10AUG81)  ************

TRANSIMPEDANCE PREAMPLIFIER

****      INPUT LISTING                          TEMPERATURE =

**********************************************************************



VCC 10 0 6.6
IIN 0 2 AC 2.E-5
CD 0 2 1PF
X1 10 2 3 HYBRID-PI
RBYP 3 4 3.3K
CBYP 3 4 10NF
RE1 4 0 1K
X2 5 4 0 HYBRID-PI
X3 7 6 5 HYBRID-PI
RC2 7 8 180
RS2 8 10 1K
CS2 8 0 10NF
RB1 6 10 3K
RB2 6 0 3.3K
CB2 6 0 10NF
X4 10 7 9 HYBRID-PI
RE3 9 0 3K
RF 9 2 3K
 .SUBCKT HYBRID-PI 1 2 3
 *NODES: COLLECTOR BASE EMITTER
RBB 2 4 31
RBE 4 5 2.2K
CBE 4 5 0.55PF
RBC 4 1 33K
CBC 4 1 0.38PF
GM 1 5 4 5 0.026
LE 5 3 5.3NH
 .ENDS HYBRID-PI
 .AC DEC 10 1MEG 501MEG
 .TF V(9) IIN
 .PLOT AC VDB(9) VP(9)
 .END
**************** ************************  SPICE 2G.5 (1

TRANSIMPEDANCE PREAMPLIFIER
****                    SMALL SIGNAL BIAS SOLUTION

**********************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  2)    0.9558    (  3)    0.9525    (  4)    0.2117

(  9)    0.4548    ( 10)    6.6000    ( 11)    0 9610

( 16)    2.9605    ( 17)    0.4542    ( 18)    0.4548
```

Fig. 4.36(a) Circuit description for pre-amplifier circuit

```
****     SMALL-SIGNAL CHARACTERISTICS

     V(9)/IIN                                  = -2.381D+03
     INPUT RESISTANCE AT IIN                   =  5.609D+02
     OUTPUT RESISTANCE AT V(9)                 =  1.130D+01
**************** ************************  SPICE 2G.5 (10AUG81)  ***************************************

TRANSIMPEDANCE PREAMPLIFIER
****                    AC ANALYSIS                                        TEMPERATURE =   27.000 DEG C

********************************************************************************************************************************

LEGEND:

 *  VDB(9)
 +  VP(9)
X
     FREQ       VDB(9)

X(*)----------------  -3.400D+01              -3.200D+01              -3.000D+01              -2.800D+01              -2.600D+0
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

X(+)----------------   0.000D-01               5.000D+01               1.000D+02               1.500D+02               2.000D+0
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  1.000D+06   -2.660D+01
  1.259D+06   -2.660D+01
  1.585D+06   -2.661D+01
  1.995D+06   -2.661D+01
  2.512D+06   -2.661D+01
  3.162D+06   -2.661D+01
  3.981D+06   -2.661D+01
  5.012D+06   -2.661D+01
  6.310D+06   -2.661D+01
  7.943D+06   -2.661D+01
  1.000D+07   -2.661D+01
  1.259D+07   -2.661D+01
  1.585D+07   -2.661D+01
  1.995D+07   -2.661D+01
  2.512D+07   -2.662D+01
  3.162D+07   -2.662D+01
  3.981D+07   -2.663D+01
  5.012D+07   -2.664D+01
  6.310D+07   -2.665D+01
  7.943D+07   -2.668D+01
  1.000D+08   -2.673D+01
  1.259D+08   -2.682D+01
  1.585D+08   -2.699D+01
  1.995D+08   -2.732D+01
  2.512D+08   -2.797D+01
  3.162D+08   -2.915D+01
  3.981D+08   -3.111D+01
  5.012D+08   -3.387D+01
                      - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
Y

          JOB CONCLUDED
           TOTAL JOB TIME            1.14
```

Fig. 4.36(b) AC simulation results

********** ********** SPICE 2G.5 (10AUG81) **********

TRANSIMPEDANCE PREAMPLIFIER
**** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

****

TIME	V(9)
0.000D-01	-1.388D-01
1.000D-10	-1.388D-01
2.000D-10	-1.388D-01
3.000D-10	-1.388D-01
4.000D-10	-1.388D-01
5.000D-10	-1.388D-01
6.000D-10	-1.388D-01
7.000D-10	-1.388D-01
8.000D-10	-1.390D-01
9.000D-10	-1.392D-01
1.000D-09	-1.399D-01
1.100D-09	-1.409D-01
1.200D-09	-1.420D-01
1.300D-09	-1.434D-01
1.400D-09	-1.457D-01
1.500D-09	-1.484D-01
1.600D-09	-1.515D-01
1.700D-09	-1.546D-01
1.800D-09	-1.577D-01
1.900D-09	-1.608D-01
2.000D-09	-1.638D-01
2.100D-09	-1.664D-01
2.200D-09	-1.686D-01
2.300D-09	-1.708D-01
2.400D-09	-1.724D-01
2.500D-09	-1.736D-01
2.600D-09	-1.748D-01
2.700D-09	-1.757D-01
2.800D-09	-1.762D-01
2.900D-09	-1.767D-01
3.000D-09	-1.770D-01
3.100D-09	-1.771D-01
3.200D-09	-1.772D-01
3.300D-09	-1.772D-01
3.400D-09	-1.772D-01
3.500D-09	-1.771D-01
3.600D-09	-1.771D-01
3.700D-09	-1.770D-01
3.800D-09	-1.769D-01
3.900D-09	-1.768D-01
4.000D-09	-1.767D-01
4.100D-09	-1.766D-01
4.200D-09	-1.766D-01
4.300D-09	-1.765D-01
4.400D-09	-1.765D-01
4.500D-09	-1.764D-01
4.600D-09	-1.764D-01
4.700D-09	-1.764D-01
4.800D-09	-1.764D-01
4.900D-09	-1.764D-01

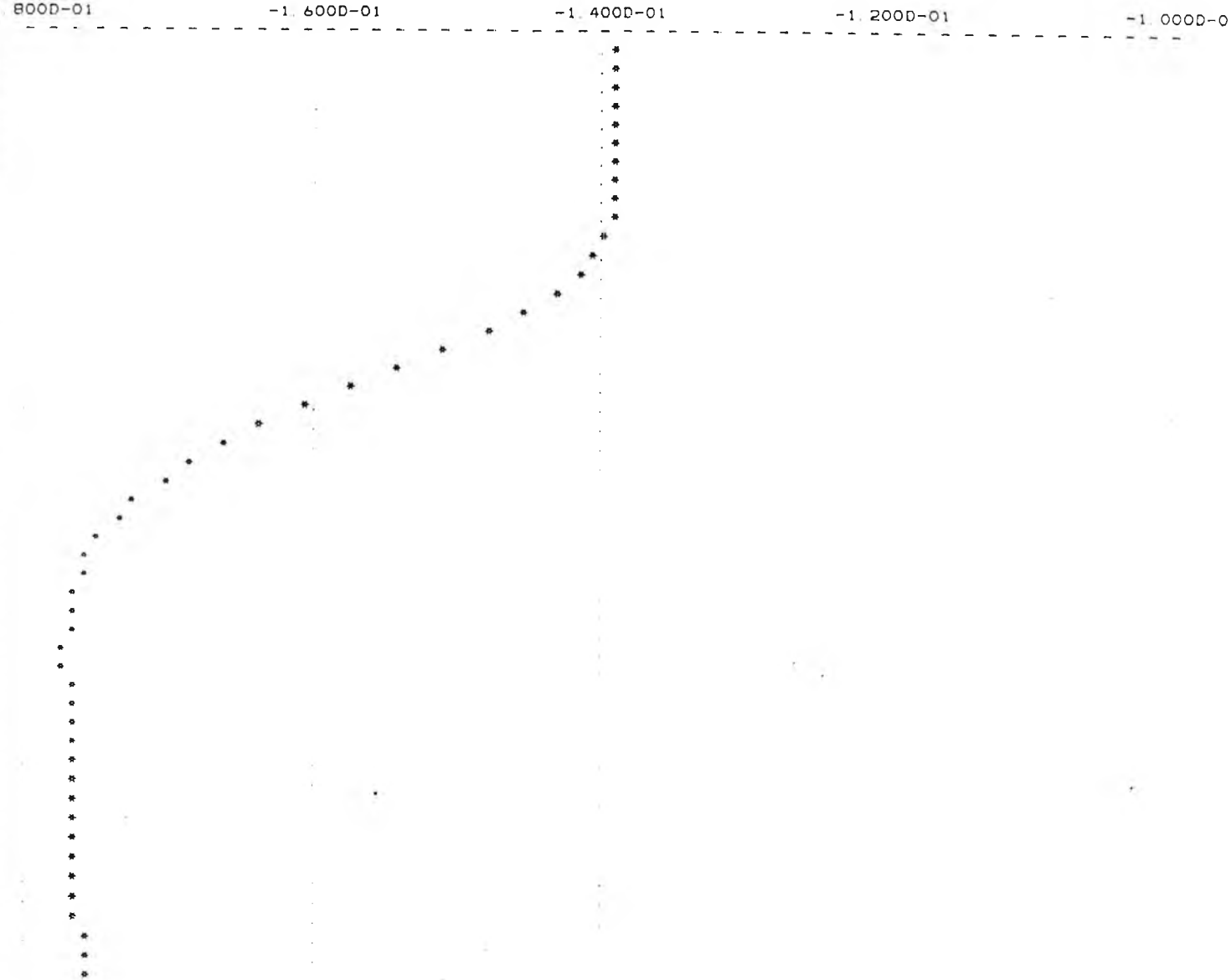
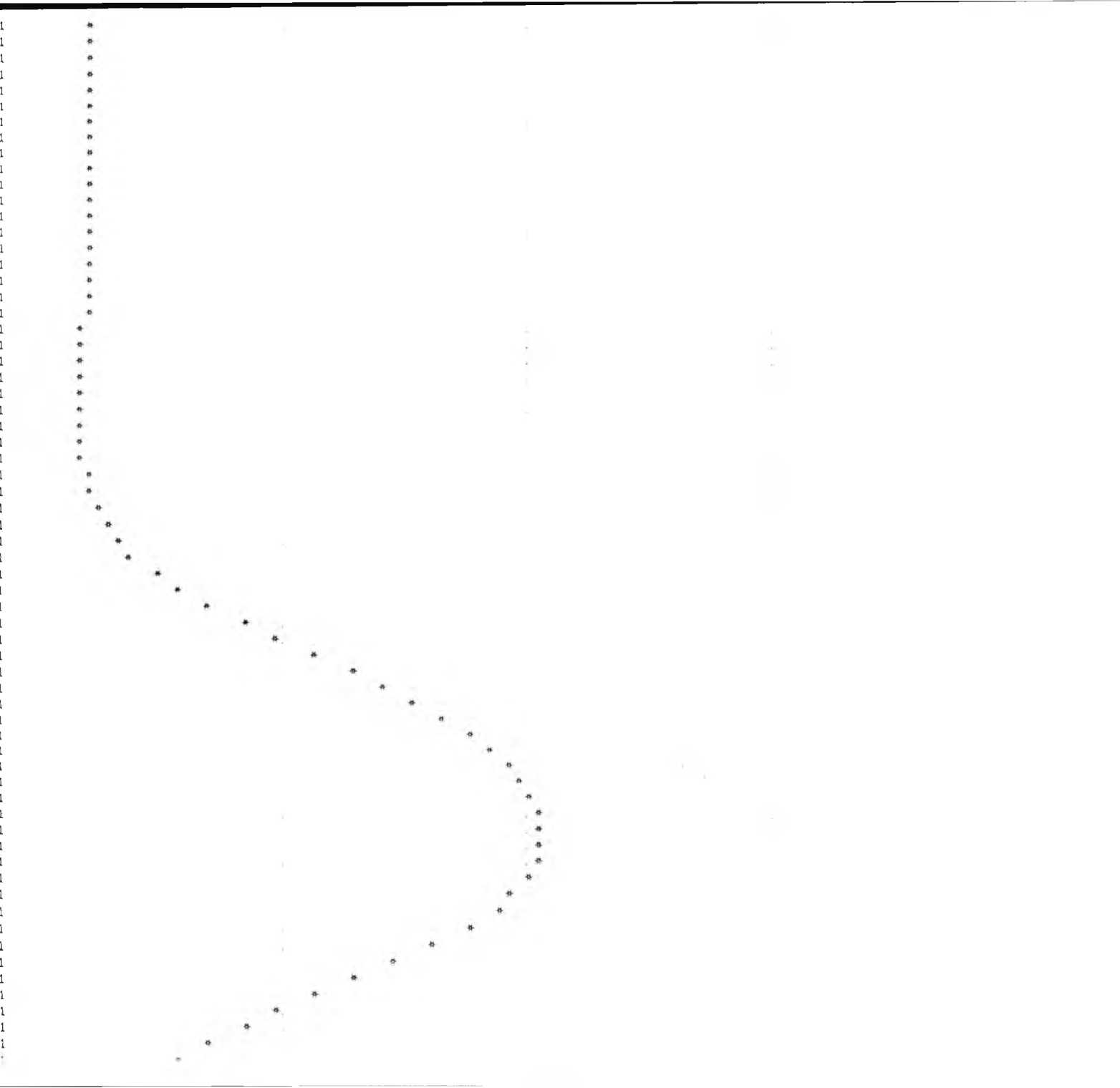


Fig 4.36(c) pre-amplifier response time

4.800D-09	-1.764D-01
4.900D-09	-1.764D-01
5.000D-09	-1.764D-01
5.100D-09	-1.764D-01
5.200D-09	-1.764D-01
5.300D-09	-1.764D-01
5.400D-09	-1.764D-01
5.500D-09	-1.764D-01
5.600D-09	-1.764D-01
5.700D-09	-1.764D-01
5.800D-09	-1.764D-01
5.900D-09	-1.764D-01
6.000D-09	-1.764D-01
6.100D-09	-1.764D-01
6.200D-09	-1.764D-01
6.300D-09	-1.764D-01
6.400D-09	-1.764D-01
6.500D-09	-1.764D-01
6.600D-09	-1.764D-01
6.700D-09	-1.764D-01
6.800D-09	-1.764D-01
6.900D-09	-1.764D-01
7.000D-09	-1.764D-01
7.100D-09	-1.764D-01
7.200D-09	-1.764D-01
7.300D-09	-1.764D-01
7.400D-09	-1.764D-01
7.500D-09	-1.764D-01
7.600D-09	-1.763D-01
7.700D-09	-1.761D-01
7.800D-09	-1.756D-01
7.900D-09	-1.747D-01
8.000D-09	-1.739D-01
8.100D-09	-1.725D-01
8.200D-09	-1.707D-01
8.300D-09	-1.689D-01
8.400D-09	-1.663D-01
8.500D-09	-1.636D-01
8.600D-09	-1.606D-01
8.700D-09	-1.576D-01
8.800D-09	-1.548D-01
8.900D-09	-1.520D-01
9.000D-09	-1.493D-01
9.100D-09	-1.470D-01
9.200D-09	-1.452D-01
9.300D-09	-1.433D-01
9.400D-09	-1.418D-01
9.500D-09	-1.406D-01
9.600D-09	-1.398D-01
9.700D-09	-1.392D-01
9.800D-09	-1.390D-01
9.900D-09	-1.389D-01
1.000D-08	-1.393D-01
1.010D-08	-1.403D-01
1.020D-08	-1.413D-01
1.030D-08	-1.427D-01
1.040D-08	-1.450D-01
1.050D-08	-1.478D-01
1.060D-08	-1.510D-01
1.070D-08	-1.542D-01
1.080D-08	-1.574D-01
1.090D-08	-1.605D-01
1.100D-08	-1.636D-01
1.110D-08	-1.662D-01
[illegible]	[illegible]

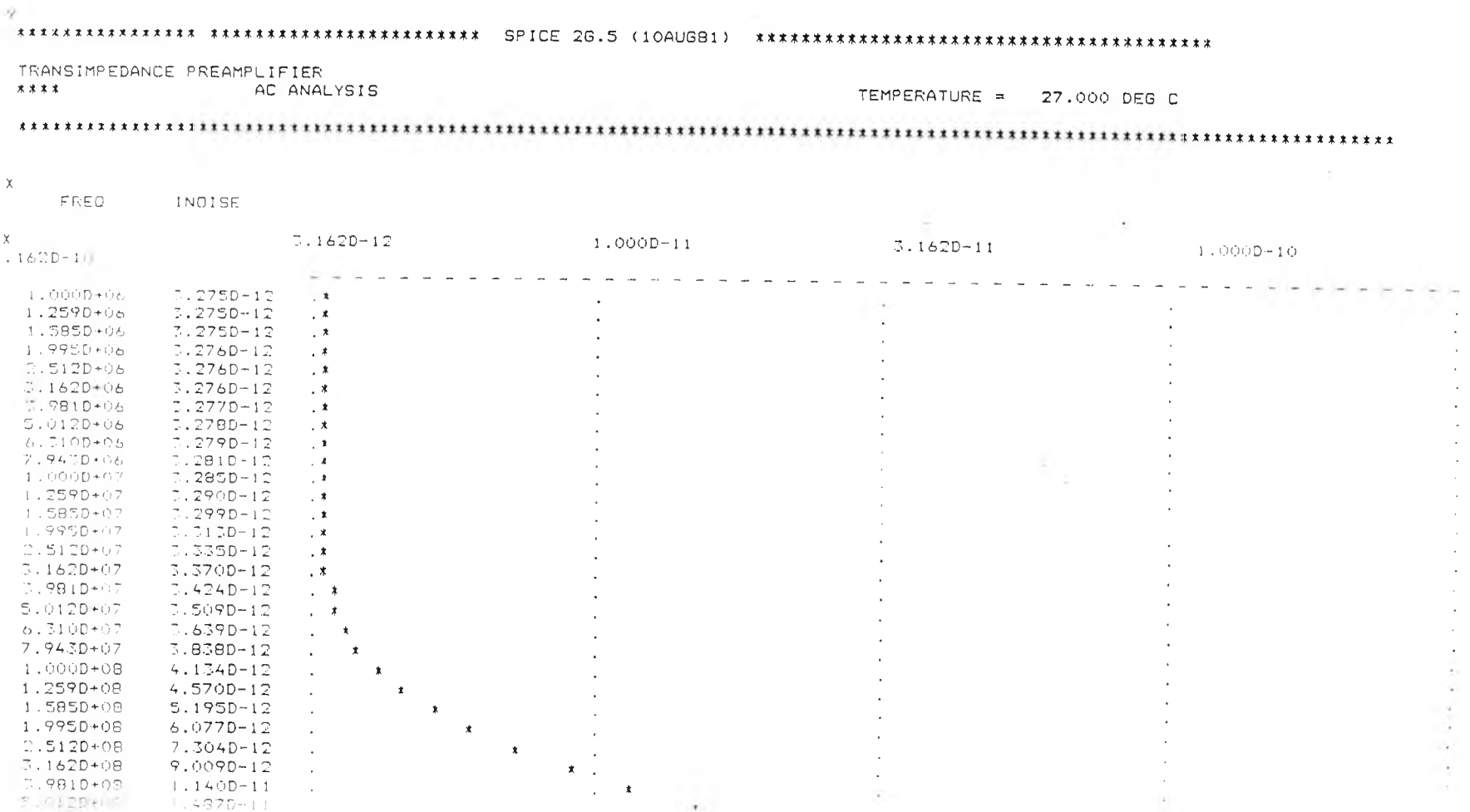


those with rectangular pulses as input to the circuit whereas sinusoid inputs are used for AC analysis.)

During the initial simulation stages of the circuit simulation, computer predictions indicated circuit instability at high frequencies. This exhibited itself as an increase in amplitude or 'peaking' at high frequencies. This could be dampened by a small capacitor across the feedback resisrtor. The value required, according to SPICE, was 1/3 pF. In practice the fabrication of this capacitor was not possible. The problem was overcome by a technique which was later found to be known as the Phantom Zero technique.

A noise analysis was also carried out to predict the noise behaviour of the circuit. At first unexpected results were obtained. SPICE predicted an improvement in the noise performance at very high frequencies where it was expected to have increasing noise levels at such frequencies. Further tests using other circuits revealed that SPICE contained an erroneous noise calculation which had to be corrected. The noise analysis shown in Fig. 4.37 is for the corrected version. This SPICE noise error and its correction were reported at a SPICE User Group Meeting.

Fig. 4.37 Noise Analysis of pre-amplifier circuit



4.6 Construction and Testing of Optical Transmitters and Receivers

The construction of the optical transmitters and receivers to be used for the optical link underwent three stages of changes during this work. On the basis of the design and analysis carried out for the driver and receiver circuits, the circuits were originally built using discrete components. By the time these have been successfully produced and tested, samples of subcircuits developed by Plessey for optical transmitters and receivers became available. These were monolithic integrated circuits packaged in leadless chip carriers (LCC). The circuits for these were designed, constructed and tested. This is covered later in this section.

The reason for this change to the Plessey components being that "standard" units must be used in the system, if it were to go into production.

Having constructed and tested the optical link using the Plessey optoelectronic components, it was revealed that these components were to be discontinued and therefore "industrially" standard replacements for the optical link had to be found.

Newly developed optical modules by BTD were found to be suitable for the application of this system.

In the following a brief outline is presented on the work carried out to construct the optical link using at the different stages.

4.6.1 Using Discrete Components

The receiver circuit was constructed using Thick Film Hybrid technology and surface mount devices. By this means stray capacitance and lead inductances are reduced to a minimum enabling higher frequency operations to achieved.

The circuit fabrication and assembly were carried by the author with the advice and assistance of Mr Keith Pitt at the Microelectronics Laboratory of the then Middlesex Polytechnic. The layout of the circuit and the artwork was produced in accordance with the design rules used for Thick Film fabrication [Pitt, 1981]. The artwork was

first produced at 20 times the actual size, then reduced to correct size for fabrication on alumina wafers. The actual size of the preamplifier was 1"×0.5" (Fig. 4.38). Fig. 4.39a shows the output of the preamplifier (lower trace) when driven by the Philips pulse generator (PM5775) output (upper trace). The fastest pulse rise time that could be obtained was that of the Philips generator which was 2.8 ns. This is not fast enough to measure the response of the amplifier which was designed to have a bandwidth of 300 MHz (rise time 1 ns). Fig. 4.39b is the same condition but with a slower time base.

4.6.2 Using Subcircuit Units

The LED driver used at this stage of the work was Plessey's SP9954 packaged in a 16 pin LCC. The receiver consisted of two units; the preamplifier, the SL9044 and the post-amplifier/comparator, the SL9944, which are packaged in 16 and 20 pin LCC respectively.

The complete link was successfully tested, but since this link was not proceeded with, the construction and testing details are not presented here.

4.6.3 Using Transmitter and Receiver Modules

In the final version of the optical transmitter and receiver of the optical link, the newly developed transmitted and receiver modules, the DLT 1000/312 and the DLR 1000/312 are used.

The transmitter module consists of the driver circuit with the optical source being an ELED operating at the 1.3μm wavelength region. Operation in this region, as mentioned earlier, results in minimum fibre loss, zero material dispersion and the LED output has narrow spectral width (resulting in less modal dispersion effect).

The receiver module consists of a PIN diode and also the pre- and post-amplifiers and a comparator which are integrated on a single wafer.

Although the electrical input to the transmitter and the output from the receiver have voltage swings compatible to ECL logic family, the modules are powered from 0V and

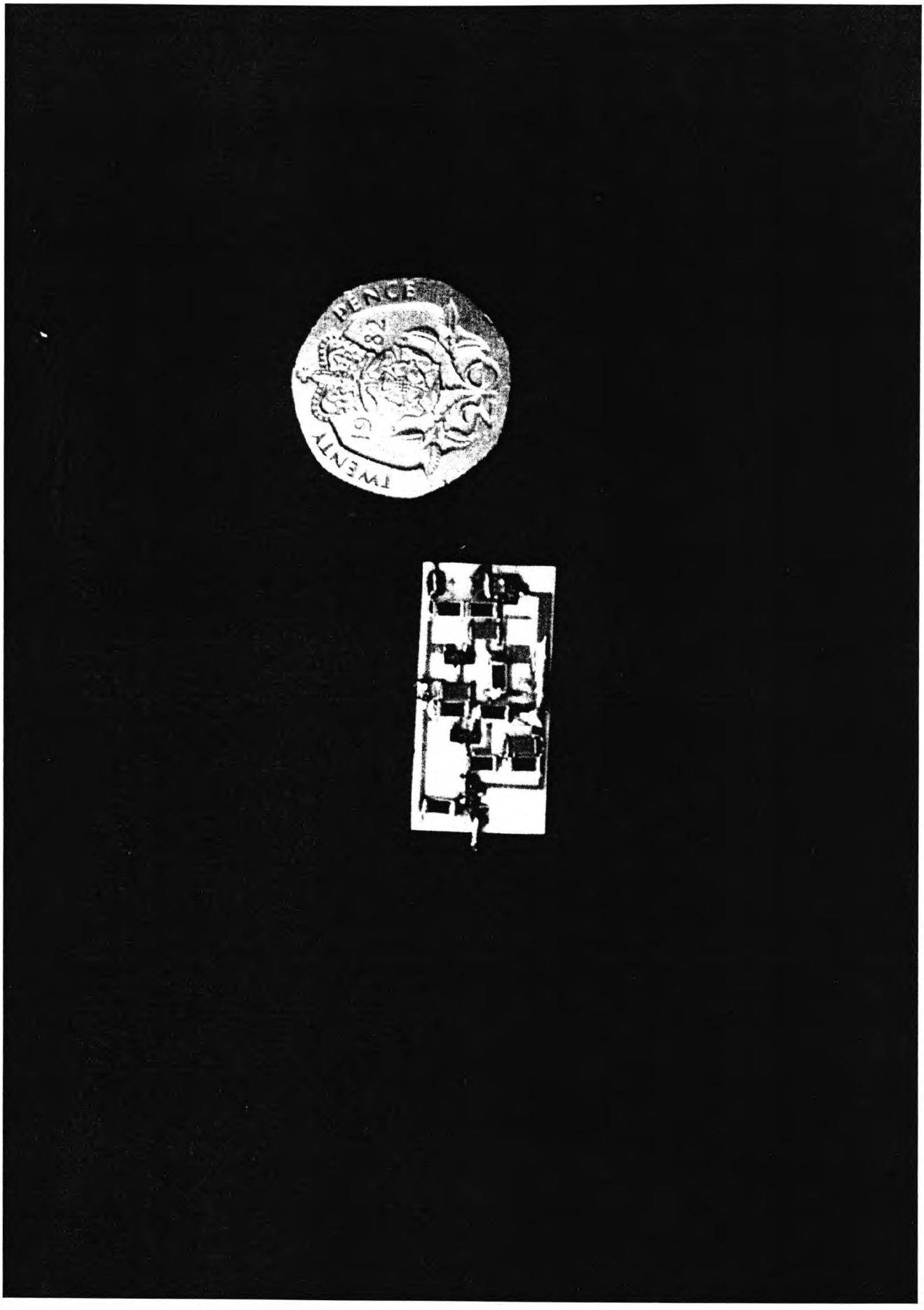


Fig. 4.38 The preamplifier circuit built on an alumina substrate using thick-film technology and surface-mount components. Scale: ×2.

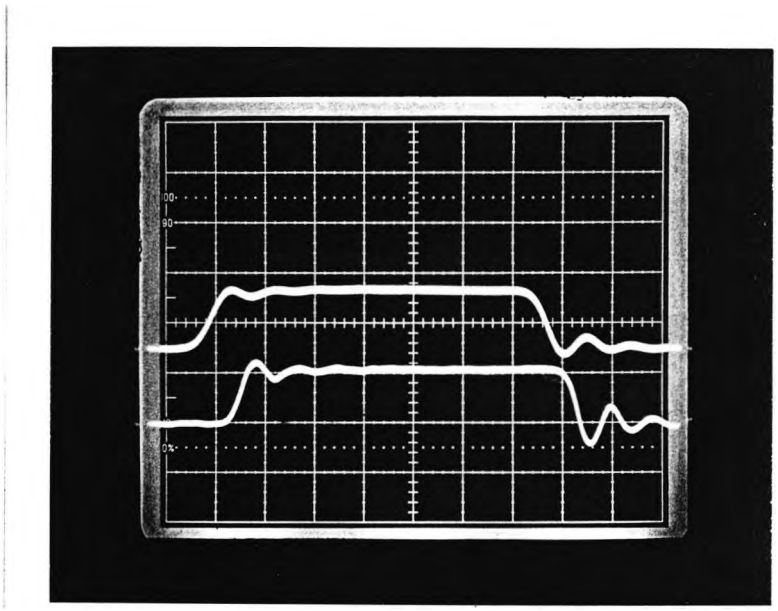


Fig. 4.39a The input (upper trace) and the output (lower trace) of the preamplifier showing the response time of the device. The scale is at 5 ns/div. The input to the preamplifier seem to have a slightly slower rise time but this is due to the loading effect of the preamplifier on the output of the generator.

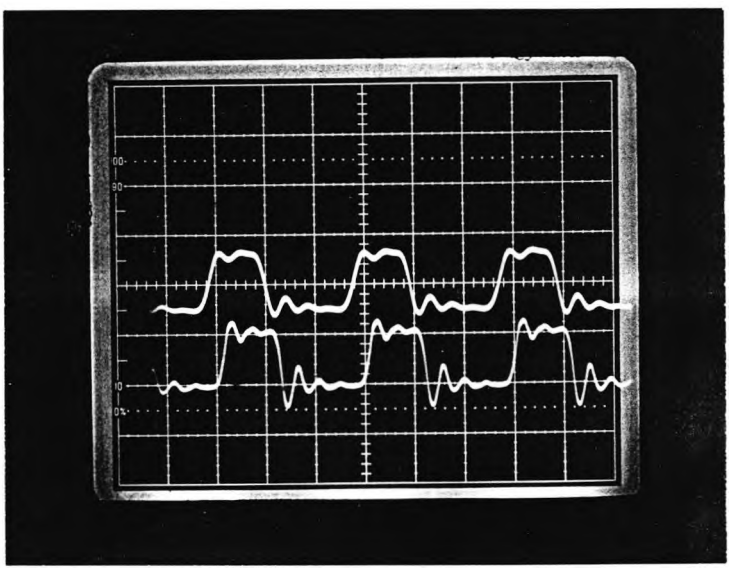


Fig. 4.39b The same as the above but with a slower time base.

+ 5V, hence referred to as pseudo ECL (PECL) logic. Standard ECL devices are powered from - 5.2V and 0V [BTD, 1990].

In this application, the transmitters are powered from standard ECL supply without any degrading effect on the performance of the driver, but the receivers are powered from PECL supply which gives better noise rejection [BTD, 1990].

With PECL, the outputs of the optical receiver cannot be directly coupled to standard ECL devices. The input voltage levels of standard ECL devices are typically -0.8V(H) and -1.7V(L), whereas the output voltage levels of PECL optical receivers are +4.2V(H) and +3.3V(L).

One way of coupling PECL devices to ECL ones is to block the dc level of the output of the PECL device and re-introduce the required dc condition for the input of the following ECL device. In this arrangement the dc levels of the receiver output are blocked at the sending end of the transmission line. At the receiving end of the cable, a pair of resistors are used to satisfy two conditions; to match the cable and to reinsert the required bias condition for standard ECL before driving on ECL devices. Calculation for this arrangement shown in Appendix A.

The output of the optical receiver (the pre-amplifier) goes into oscillation in the absence of input signal [BTD, 1990]. A Signal Detect (SD) output indicates the presence of a signal (above a specific threshold [BTD, 1990]) by going high. In order to prevent the oscillation from driving the subsequent circuits, the receiver output is blocked by ANDing it with the 'SD' output. Series termination is used at the sending end of the transmission line connecting the optical receiver output and the AND gate inputs which eliminates the need for a matching circuit at the receiving end of the line. This is used for matching the line to prevent any distortion to the signal. On the other hand, parallel termination is used at the receiving end of the line connecting the decoupled output of the AND gate and the input of devices powered to standard ECL.

By this means we not only match the line at the receiving end, but also provide the bias level necessary for correct operation of the standard ECL devices.

4.7 Summary

The various components and circuits of a fibre optic link were reviewed with emphasis to its application in such a system as the DOCTR system.

Amongst the three types of fibre optic cables, the multimode graded index fibre is most suitable for the application of this work. This type of fibre exhibits good coupling efficiency without suffering from high levels of intermodal dispersion.

LEDs were selected as the optical source because of their reliability and drive circuit simplicity. The features of the laser diodes were not essential for this application. For similar reasons, the PIN PD was preferred to APD.

The circuits for the transmitter and receiver were designed to provide optimum performance. For the circuits using discrete components, device characterisation was accomplished in order to achieve accurate simulation results.

The digital FOL unit was consecutively constructed in three different technologies during this work. The final version of the FOL unit underwent various tests which will be discussed in chapter 6. The FOL unit consists of 9 channels through which data is transmitted in parallel. Particular consideration was taken to ensure negligible path differences between the individual channels. The recording unit of the DOCTR system is particularly sensitive to path differences. This is because of the high speed of operation of the system where data is transmitted and recorded at a rate of 100 MS/s and the recording signal has a pulse width of 5 ns.

CHAPTER 5

RECORDER UNIT

5.1 Introduction

The recorder unit is the second half of the DOCTR system and is situated in a relatively interference-free zone, but coupled to the signal capture unit by the fibre optic link. It is made up of two sub-units which have different functions. The sub-units are:

* the optical receivers (of the optical link);

* the RAM bank and its control circuits

The optical receivers convert digital optical signals back to electrical ones which are then processed by the control circuit. Under the influence of the control circuit the required data is stored in the RAM bank and once full, the latter is interrogated by the computer through the interface circuit. The optical receivers were described in detail in

unit and its control circuits. It discusses all aspects involved in its synthesis and analysis of the recorder unit circuits, starting from the specifications required for the recorder unit and the RAM bank within the unit, to details on speed, response and propagation delay of the different components used in the control circuits. A brief history of previous work on the control circuit designs for different versions of the RAMs considered in the project is also presented. The simulation results are discussed towards the end of the chapter.

5.2 Functional Specification of the Recorder Unit

The recorder unit is to record incoming digitised sampled data of *random* transients, but because of the unpredictability of their arrival and also since no pre-triggering facilities are to be used, data is continuously written into the RAMs and subsequently over-written until the RAMs are "triggered" by a circuit which continuously monitors the status of the incoming data. By this means a specific record is kept, determined by a preset condition. It is therefore necessary to be able to recognise the signal so that it can be recorded in the RAMs. A detection circuit is used to indicate the presence of the signal to be recorded so that the corresponding data is saved while the unwanted data is over-written.

There are circumstances where the data prior to the *event* may also be required for analysis etc even though it is not part of the main signal data. For this purpose a circuit is used which can be programmed to set the required length of the pre-event data to be kept.

The aim of the control circuit in the recorder unit is to synchronise the setting up of the data and address lines at the corresponding inputs of the RAMs prior to the arrival of the write pulse. The minimum write pulse width plus the 'set up' and 'hold' times determine the maximum writing speed into the RAMs.

5.3 The Random Access Memory

Continuous advances in the state-of-the-art technology meant that new devices with higher specification rating than their predecessors become available by the time the former were due to be implemented in a particular design. The case of the random access memories required by the recording unit of the DOCTR is no exception.

In the ultra high speed range, the writing speed and the cell array organisation (mbits x nwords) of the RAMs were lower at the start of the work on this project than they are now. The speed and organisation of the RAMs first considered to be used for the recording unit meant that 16 RAM devices were required for the project, and the corresponding circuits were designed to accommodate this. Later, higher capacity RAMs became available which, as a result, cut the number of the RAM devices required to 8. Subsequently the circuit and layout for these RAMs were designed in order to be implemented for the recorder unit. More recently the state-of-the-art GaAs based RAMs became available which, with the speed and organisation that they have, makes it possible to use only 2 of these devices for the recorder unit. The final recorder unit is based on these devices and in the next section of this chapter, design details of the RAM control circuit will be presented. However, an outline of the design of circuit based on the previous versions of the RAMs is given in this section. It should be noted that with the progress in the developments of high speed, high capacity RAMs, such devices have, at the time of writing, become available which have a similar speed, but a much still capacity than the final RAM mentioned, on a single chip.

5.3.1 Interlaced RAMs

The high speed RAMs which were commercially available when the work on this project began were not capable of recording at rates of 100 MS/s. The required sampling rate for the ADC was 100 MS/sec and if a digital record of the output of the ADC were to be kept, it was essential to be able to record the digital data at the same rate as it was being generated i.e. 100 MS/sec. The only practical option was to use an interlaced system of RAMs where the incoming data is demultiplexed between two

RAM sets . In this case the recording rate of each RAM set need only be half of that of the ADC sampling rate.

The first type of RAMs used were Fairchild's F100415 ECL RAM [Fairchild, 1985] and had a 1024 words by 1bit (1K x 1bit) organisation and therefore for parallel recording of the eight bits of a sample we needed 8 RAMs to give the required storing capacity of 1K x 8bits for each set of RAMs for the interlaced system.

In an interlaced system the incoming data is "switched" between the two RAM sets. The circuit used to demultiplex the incoming data between the RAMs is shown in Figure 5.1. The outputs of each group drive one of the RAM sets at a rate of one sample every 20 ns giving a recording rate of 50 MS/s. The arrangement for the one set of RAMs is shown in figure 5.2 and that for the demultiplexing gates is shown in figure 5.3. The complete block diagram for the RAM unit is presented in figure 5.4.

5.3.2 Using the VS12G422E RAMs

The next RAM which was considered for the project was the newly arrived VS12G422E [Vitesse, 1988]. The reason for changing to these RAMs was their high speeds allowed by their 3 ns write pulse width which meant that we no longer needed to use interlaced RAMs to record data at a rate of 100 MS/sec. (The 3 ns pulse width plus the data and address 'setup' and 'hold' times added to less than 10 ns, allowing data to be written into the RAM during that period.) These RAMs are organised for 256 words by 4bits meaning that we can use eight of them to achieve our minimum record length of 1024 words by 8 bits. No data demultiplexing is required with these RAMs, but since the record length of each RAM is only 256 words, we need to use four of these RAMs in series to get the 1024 word length. The circuit design also needs to dictate which RAM is enabled at any time during the write period. The VS12G422E units have eight address inputs (A_0-A_7) and therefore only the eight least significant bits of the 10-bit address-generating counter are used to address the RAMs and the other two, the most significant bits A_8-A_9 are used to drive a decoder circuit to select

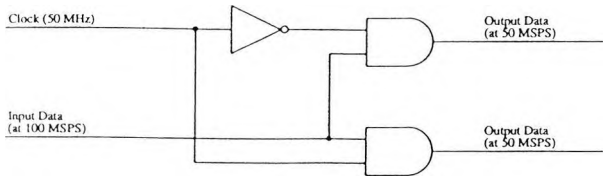


Fig 5.1 Demultiplexer circuit for interleaved RAM circuit

The data inputs are driven through the demultiplexer outputs

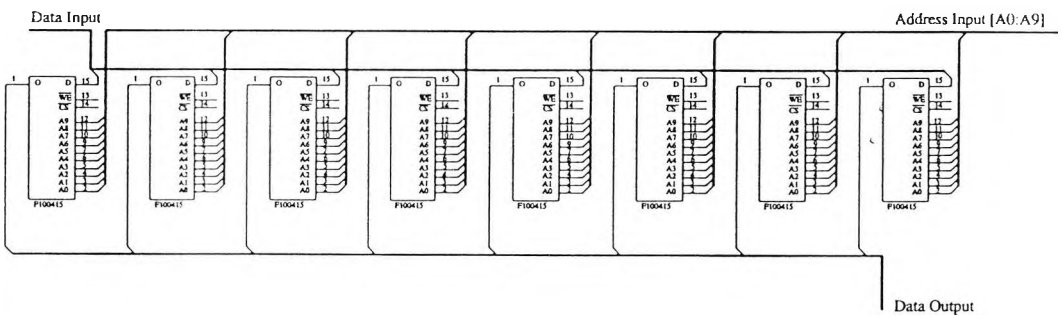


Fig 5.2 One set of RAMs for interleaved system

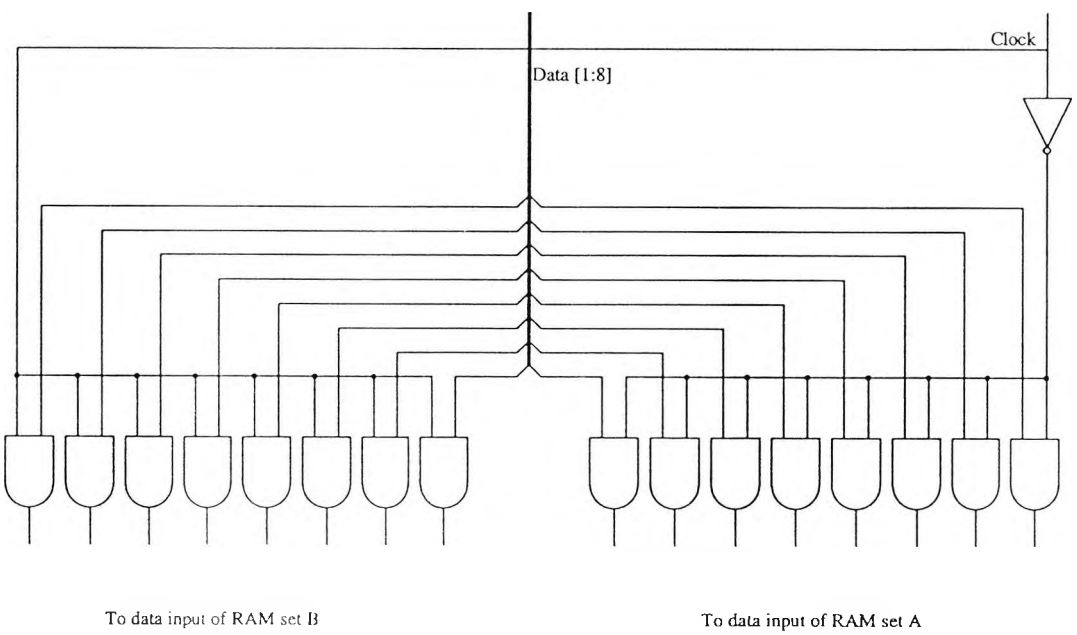


Fig 5.3 Demultiplexing gates circuit

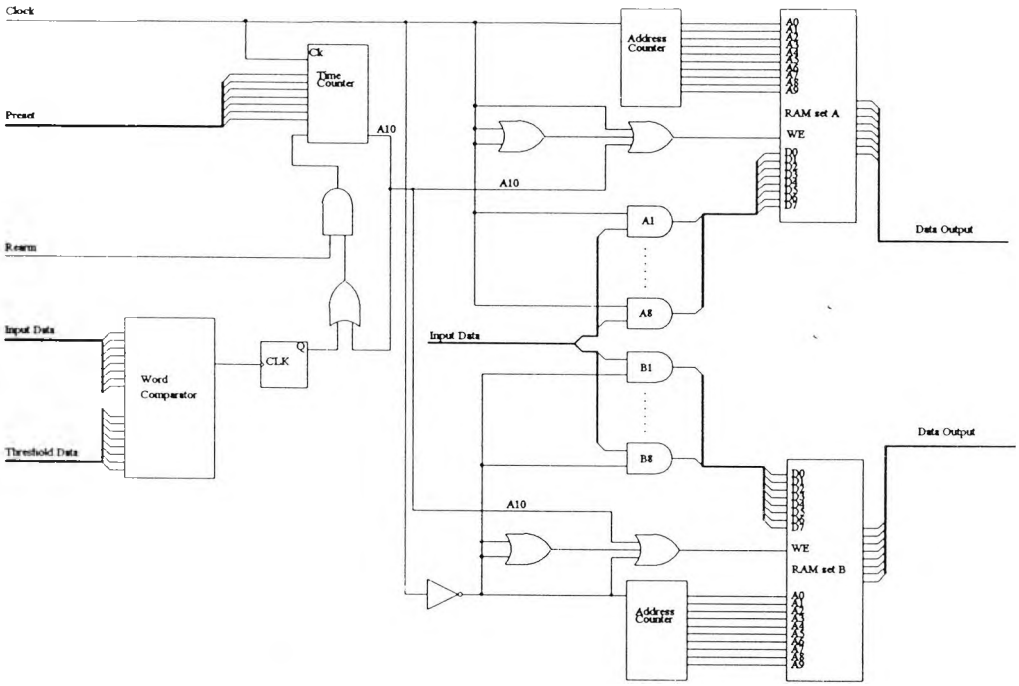


Fig 5.4 Block diagram for interleaved RAM system

a particular RAM during the read/write periods. The decoder circuit design is shown in figure 5.5 together with its truth table. As can be seen from the truth table, for the 256 address locations, RAM1 is selected while others are disabled. Similarly for the second, third and fourth 256 address locations RAMs 2, 3 and 4 are individually selected respectively.

The complete block diagram for the RAM unit is given in figure 5.6. The layout for the RAM circuit are shown in figures 5.7.

5.3.3 Using The VS12G47 RAMs

The VS12G47 is another ultra high speed static RAM with writing speed of less than 3 ns [Vitesse, 1989] but it has a higher storage capacity than that of the VS12G47E. It is organised for 1024 words by 4 bits (1K x 4) and therefore only two of these RAMs are required to store 1024 eight-bit samples. Furthermore, with these RAMs no external decoder circuits are necessary for 1K x 8 capacity. The two RAMs are used in tandem so that the same address generator drives the ten address inputs of each RAM simultaneously. Similarly the same clock source drives the clock inputs of both RAMs in synchronism. However, only half of the 8 bits of a sample feed into the data inputs of one RAM and the other four bits feed the second RAM. If more storage capacity were to be required, extra tandem pairs could be added to the existing RAMs. The detailed design discussions are given later in this chapter.

The VS12G47 static RAM has five input sets as follows:

address inputs A_0-A_9

data inputs D_0-D_3

clock input CK

read/write WE

chip select CS

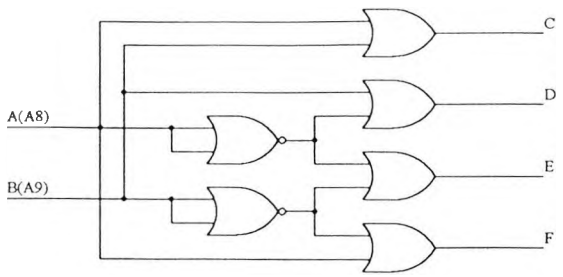


Fig 5.5 Address decoding circuit generating bit select outputs

B	A	C	D	E	F
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	11	1	0

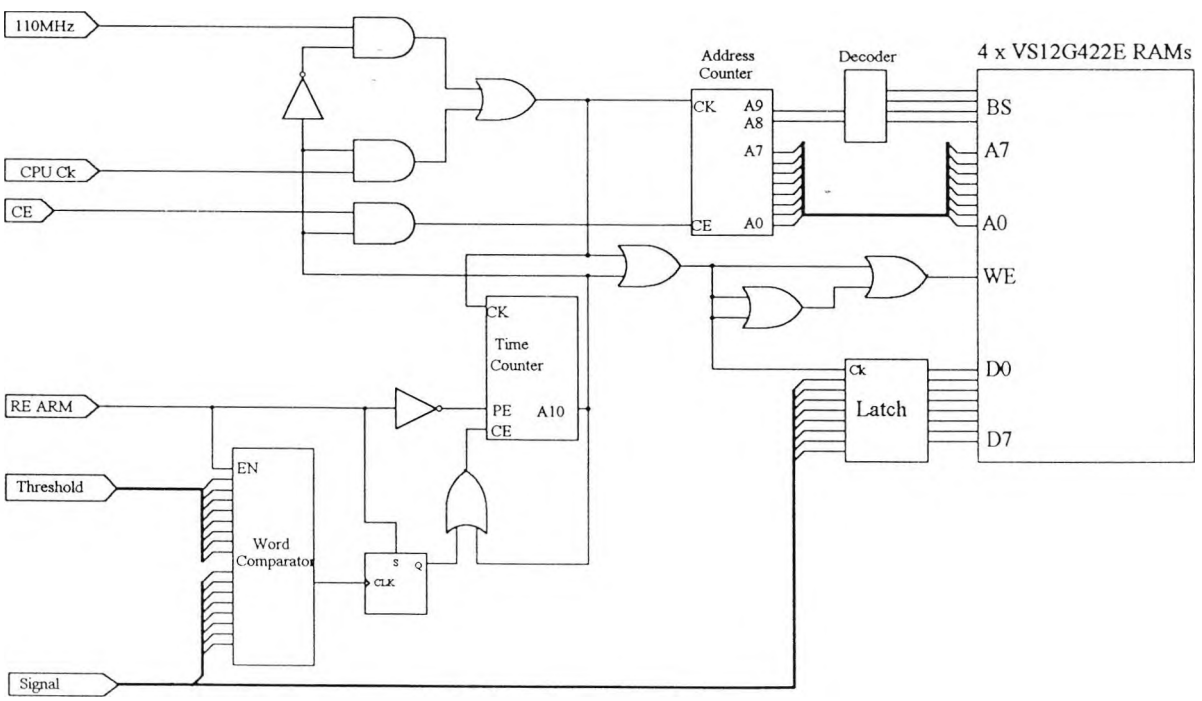


Fig 5.6 Circuit for VS12G422E RAMs

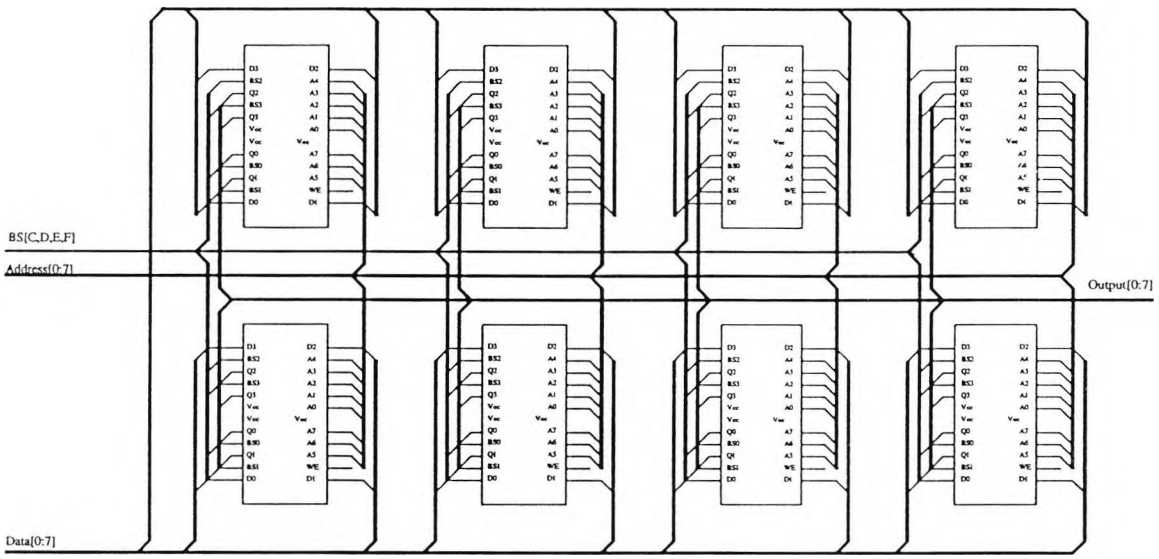


Fig 5.7 Layout for the VS12G422E RAM ICs

An address generating circuit drives the ten address inputs of the RAM while the data to be recorded is set up at the data inputs of the RAM. The control of the flow of data into the RAM and its modes of operation are determined by the input signals CK, WE and CS.

The CK signal is used to clock in the data that is set up at the address and data inputs of the RAM. The WE signal determines the mode of operation of the RAM i.e. to Read or Write . The CS signal is used to enable or disable a particular RAM when a number of them are used in a circuit and only one must be operational at any one time. In this project, since only one tandem pair of RAMs is used, there is no need to use the CS and it is kept at logic low permanently.

5.4 Design of the RAM Control Circuits

The function of the RAM control circuit is to control the signal and address data at the inputs of the RAMs, taking into account the 'setup' and 'hold' times required before the data is clocked in. In addition, there are two further functions to be accomplished by the circuit which are specific to this application. First a signal monitoring circuit is used to "trigger" the recording unit in the presence of a required transient signal so that the corresponding sample data is not overwritten. Second, the control circuit also allows the immediate "pre-trigger" history of the signal concerned to be recorded and the circuit for this function is driven by the signal monitoring circuit mentioned above. The designs for these circuits as well as other sub-circuits are outlined in the following sections of the chapter.

5.4.1 Setting up the address and data lines

The address data for the RAMs are generated by a 12-bit address generating circuit which is made up of three cascaded 4-bit counters as shown in figure 5.8. The 4-bit counters in the final design of the control circuit are Motorola's MC10H13 [Motorola, 1986]. All previous designs of the control circuit had been based on Motorola's MC10H016 4-bit counters [Motorola, 1986], but these have become obsolete.

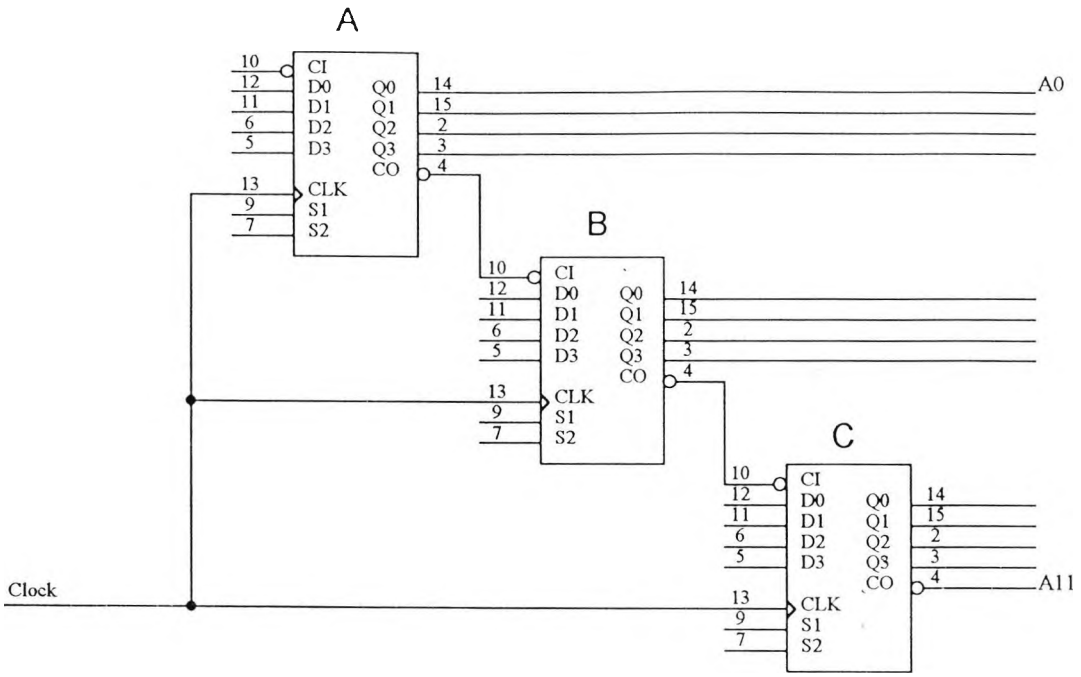


Fig 5.8 Address generator

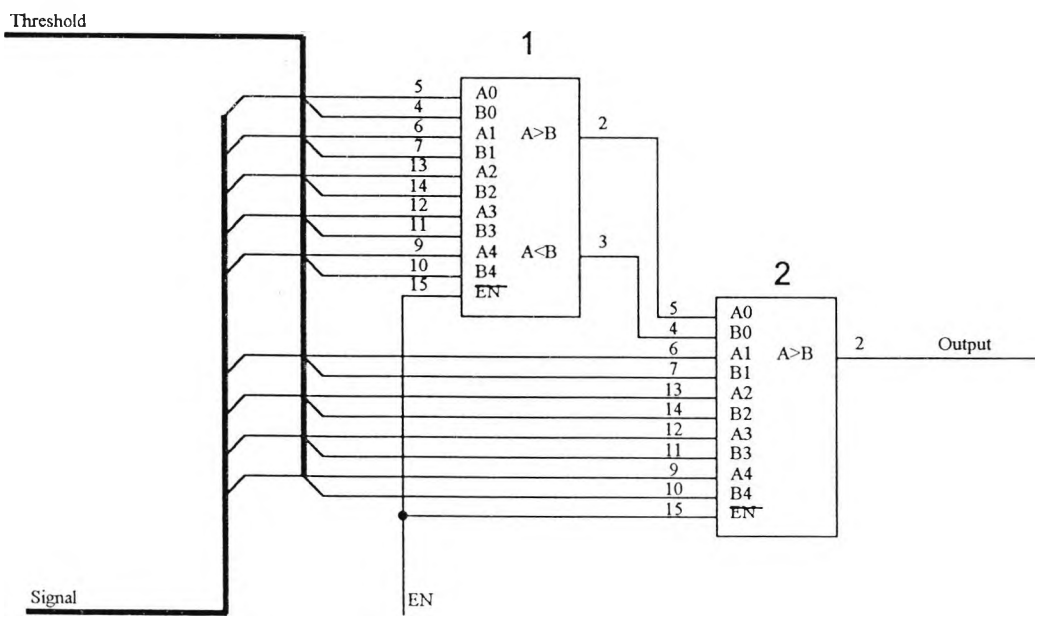


Fig 5.9 Signal Monitoring Circuit

Although a few of these counters were available, it was considered prudent to base the design on components which are commercially available. Therefore the control circuit had to be redesigned to accommodate the new counter.

The counter is disabled when the input C_{in} is at logic high and enabled when low. On terminal count (or the final count of the counter) the output C_O goes low and therefore in a multistage counter (such as the 12-bit counter) when counter A reaches terminal count, its C_O enables the next counter (B) and at the next clock pulse counter B will be incremented as well as counter A. At this stage, C_O of counter B will go high, disabling it until the next terminal count. [Motorola, 1986]

Only the first 10 bits [A_0_A_9] of the output of the 12bit address circuit will be used to drive the RAMs address inputs.

The signal data is first latched into an octal latch before it is set up at the RAM data inputs [Motorola, 1986].

The address generator and the octal latch are both driven by the same phase of a clock resulting in the address and signal data being set up at the RAMs inputs ahead of the "writing" phase of the clock. Due to the different propagation delays of the address counter and the octal latch, the address and signal data will be output at different times with respect to each other. To conform with the 'setup' time requirements, a clock signal which is out-of-phase with that driving the address generator and latch is used to write the data into the RAMs Fig 5.13(a). This allows all the address and data signals to be 'setup' at the corresponding inputs of the RAMs before the arrival of the 'write' clock signal.

5.4.2 Signal Monitoring Circuit

The Signal Monitoring Circuit (SMC) is made up of two 5-bit word comparators [Motorola, 1986] and a D-type flipflop to monitor the status of the signal being recorded. With such a circuit, the user is able to set a threshold level to be used as a

reference by the SMC. Any signal level below that of the threshold level will be ignored by the SMC, whereas the latter will "trigger" the recording unit when a signal level greater than that of the reference is detected. This feature may be used to allow for any (background) noise in the measurement when a signal is noisy.

A nine-bit word comparator is achieved using two 5-bit word comparators as shown in figure 5.9.

The outputs of comparator 1 drive into the LSB inputs of comparator 2 resulting in a 9-bit word comparator with its outputs being those of comparator 2. The output of 9-bit comparator drives the following flipflop. During the operation of the system, in the presence of a signal greater than the threshold level, the comparator flags the status of the signal and this is latched into the flipflop. In turn the flipflop enables the pre-trigger circuit (discussed in the next section) which, depending on the number of pre-trigger samples programmed into the circuit, will stop the recording into the RAMs and switches the operation mode of the RAMs from write to read. Another function of the pre-trigger circuit is to initiate the computer to retrieve the data from the RAM bank. Before re-arming the recording unit for further recordings, the software developed to control the operation of the recorder unit prompts the user for new threshold level and pre-trigger settings.

5.4.3 Programmable Pre-trigger Circuit

Sampled data is continuously written into the RAMs and is overwritten during the next cycle unless the Signal Monitoring Circuit (SMC) is activated. It does this upon the detection of the presence of the signal to be recorded and thus triggers the "pre-trigger" circuit so that the specific data in the RAM bank is not overwritten The pre-trigger circuit is programmed to determine the recording period and therefore the number of "pre-trigger" samples to be monitored. The pre-trigger circuit is made up of a 12-bit counter into which the number of pre-trigger samples are loaded . When the recording system has been re-armed by the computer, the pre-trigger circuit is set in

'hold' mode and no further action is taken by this circuit. At this stage signal data is continuously written into the RAMs and subsequently overwritten. This continues until the SMC detects the signal to be recorded which in turn clocks the flipflop to enable the pre-trigger circuit. Depending on the required record length of the signal prior to the trigger event, the pre-trigger circuit will inhibit the RAM bank unit from recording and set the latter into Read mode to allow the computer to retrieve the data from the RAM bank. The speed of data retrieval does not have to be the same as the writing speed (100 MS/s), but as fast as the computer bus operates. Once all the data has been transferred to the computer, the latter prompts the user to set the new trigger threshold level and the pre-trigger samples to be recorded.

5.4.4 The TTL-ECL Translators

The interface circuit between the control unit and the PC is built using TTL technology, since it is not operated at high speeds and ECL technology is not required.

The trigger threshold level and also the number of pre-trigger samples which are set by the user are output in TTL technology (by the computer via the interface circuit) and are translated to ECL using the TTL-ECL translators (Motorola's MC10124). The data is first stored in separate octal latches, the outputs of which directly drive the translators. Similarly the RAM outputs are read by the interface circuit through ECL-TTL translators. The control lines from the PC to the RAM control circuit and the flag signal from the control circuit are all passed through the appropriate translators.

5.4.5 Matching ECL-Output To GaAs-Input

The static RAMs being used in the recording unit has an access time of less than 3 ns making it one of the fastest RAMs commercially available in the market (at the time of purchase of these devices) as well as the having adequate storage capacity for such speeds. This speed is achieved by using the III-V family of semiconductors (Gallium-Arsenide (GaAs)) which exhibit properties enabling very high clocking speed to be applied to the device compared with those that may be applied to Silicon (Si) based

devices. GaAs based devices have different energy levels to those which are Si based and although the manufacturers of the VS12G74 claimed that these RAMs may be used in ECL board environments [Vitesse, 1989] closer study of the input and output voltage range levels of the VS12G74 and standard ECL devices indicates that these two families are not always compatible. The chart illustrated in figure 5.10 shows the degree of incompatibility between these RAMs and the other devices used in the rest of the control circuit which are of standard ECL technology. The following are observed from the chart of figure 5.10:

ECL output driving GaAs input: (left half of chart)

At the HIGH logic level the ECL output voltage range falls within the GaAs input voltage range which is satisfactory. However, at the LOW logic level the ECL output voltage range is not within the GaAs input voltage range and the former only partly overlaps with the latter. This is not acceptable for the correct circuit operation.

GaAs output driving ECL input:

At both the HIGH and the LOW logic states the GaAs output voltage range does not completely overlap with the ECL input voltage range.

It is therefore important to arrange for the input and output voltages of the two technologies to be within acceptable levels to ensure correct operation of the RAM bank circuits.

The following arrangement is used to facilitate the coupling of ECL output to GaAs input:

The standard ECL output is an open emitter [Motorola, 1986] enabling it to drive matched transmission lines of any impedance. In the absence of a transmission line, a pull down resistor must be used. In the case of ECL-GaAs interface, a resistive divider may be used to shift the d.c. voltage levels at the ECL output down so that the ECL output voltage range falls within the GaAs input voltage range. With reference to the

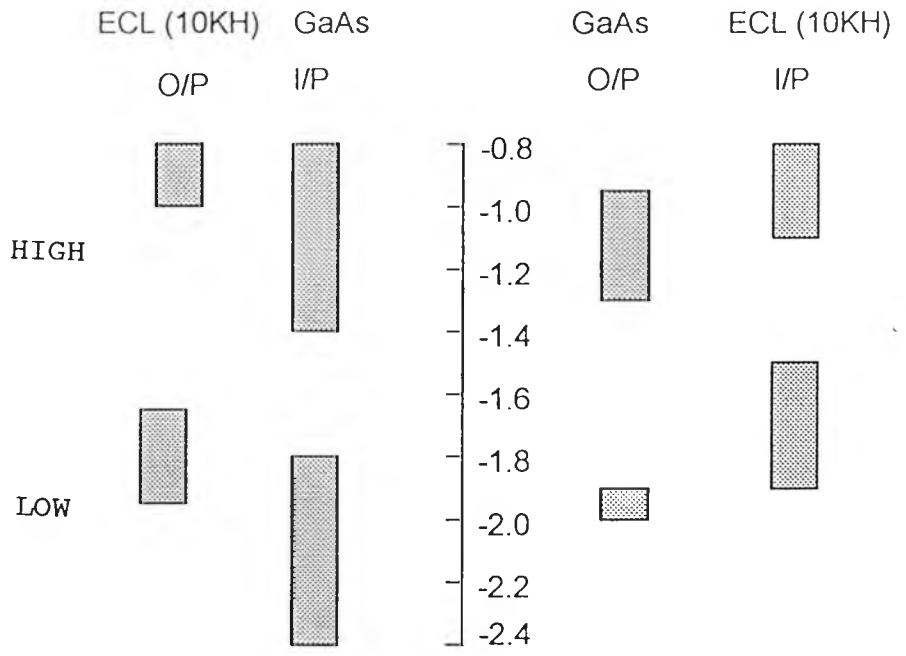


Fig 5.10 ECL and GaAs RAM input/output voltage ranges

chart of figure 5.10, the minimum voltage swing of the ECL output (or the width of the transition region) is about 0.6 Volts and that of the GaAs input is 0.4 Volts. Therefore if the ECL output is to be equally symmetrical around the GaAs input voltage range, there will be a total of about 200 mV noise margin for each of the HIGH and LOW logic states. The proposed method is depicted in figure 5.11.

The calculations for this circuit are given in Appendix B.

In the case of interfacing the GaAs output to ECL input, since the GaAs output needs to be shifted up in the positive direction (see figure 5.10) we cannot use resistive dividers for this purpose. We will, therefore, use decoupling capacitors at the output of the GaAs device and use resistive termination at the end of the line to both match the line and restore the d.c. level required for standard ECL. This is shown in figure 5.12.

The block diagram for the recorder unit is shown in Fig 5. 13(a) and the complete circuit for the recorder unit including the receiver circuit for the unit is shown in figure 5.13(b).

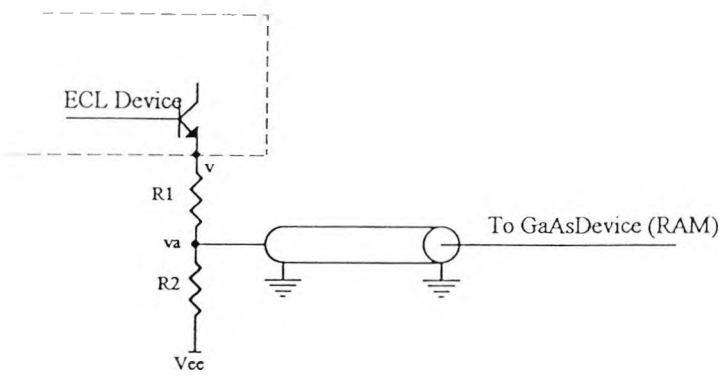


Fig 5.11 ECL-to-GaAs matching circuit

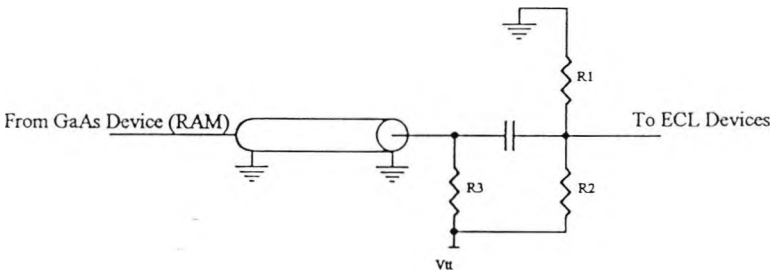


Fig 5.12 GaAs-to-ECL matching circuit

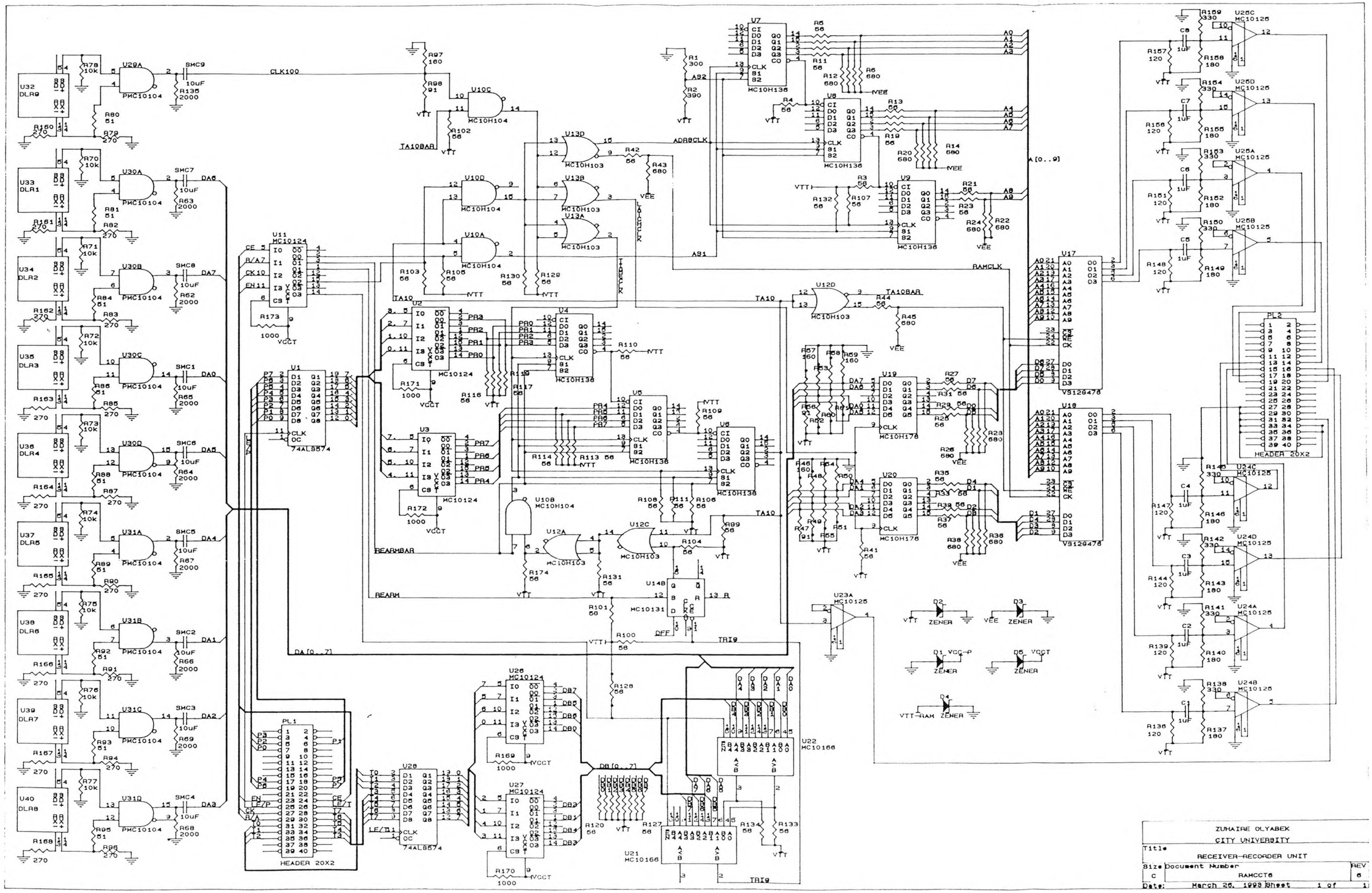


Fig 5.13(b) Complete Circuit Diagram of Recorder Unit

5.5 Simulation of the Recorder Unit

The simulation program used to analyse the behaviour of the recorder unit was the System HILO 4 which is one of the leading digital circuit simulation packages. It allows the user to create a circuit file and a waveform file. The circuit file describes the various devices used within the circuit. It also outlines the interconnections of these devices as well as the input and output ports. In the waveform file the signals or waveforms which drive the hardware circuit are described. Various types of (input) waveforms and their individual characteristics may be defined in the waveform file.

The waveform file is used by System HILO to drive the circuit file and the resultant waveform outputs at the specified nodes are displayed. The type of output display and the nodes to be monitored are specified in a separate file.

In high speed digital devices the main two features which characterise the device are the rise/fall times and the propagation delay through the device. The propagation delay is defined as the time taken for the device output to stabilise in response to a given input. The task of the circuit design is made more difficult when these two features become comparable to the clock cycle or the period of the pulse driving the circuit. The difficulty is increased when various devices are used and each device has a 'range' of values for its propagation delay. The accumulation of the various ranges of propagation delays must be carefully analysed in the high speed circuit designs. The design of such circuit taking into account the best and worst cases becomes extremely difficult. In fact it is this wide gap between the best and worst case which determines the limits to the performance of memory circuits. The task of the control and monitoring circuits is to ensure that the address and signal data are 'set up' and 'held' correctly with respect to the 'write' pulse. For a recording rate of 100 MS/s, the clock cycle is 10 ns and the write pulse width is 5ns.

5.5.1 Inputs to HILO

The circuit file is written using Genrad's Hardware Description Language (GHDL) and the waveform file is written using the Wavefrom Description Language (WDL). Typical circuit and waveform files are given in Appendix C.

5.5.2 Output of HILO

The output of the simulation of Fig 5.14 shows how the data and address signals are set up prior to the rising edge of the "write" pulse (called the RAMCLK in the WDL program). This simulation result confirms the validity of the design for the control and monitoring circuits. It can be seen that the inputs to the RAMs, i.e. the address and data signals, are established prior to the arrival of the clock (RAMCLK) signal. This satisfies the setup requirements for correct operation of the RAMs [Vitesse, 1989].

The re-arming of the recorder unit by the PC, which is done once the recorded data has been retrieved from the RAMs, has been confirmed. Also in this analysis, the operation of the signal monitoring circuit as well as that of the programmable pre-trigger circuit have been confirmed. The results of these operations are not shown in the timing diagram.

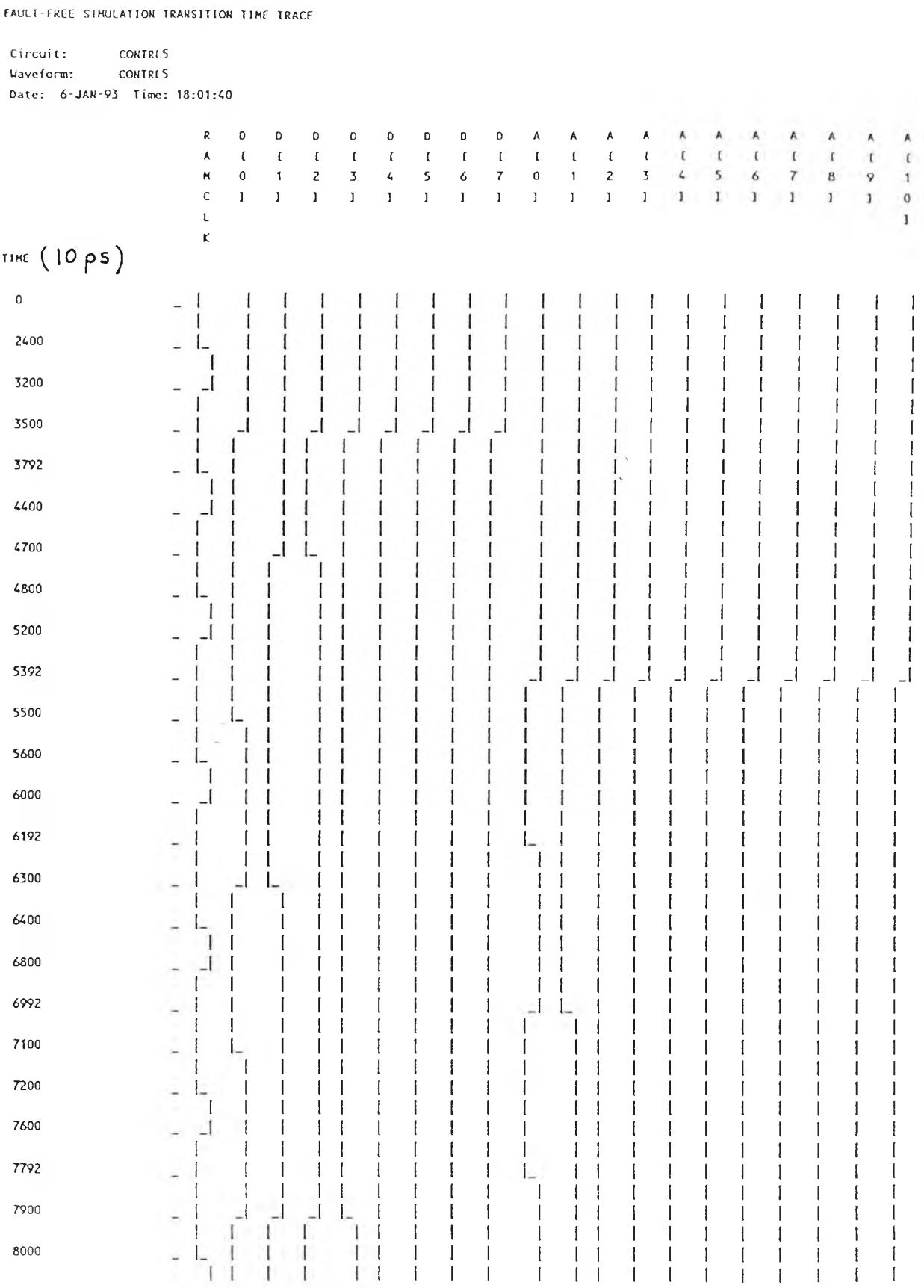
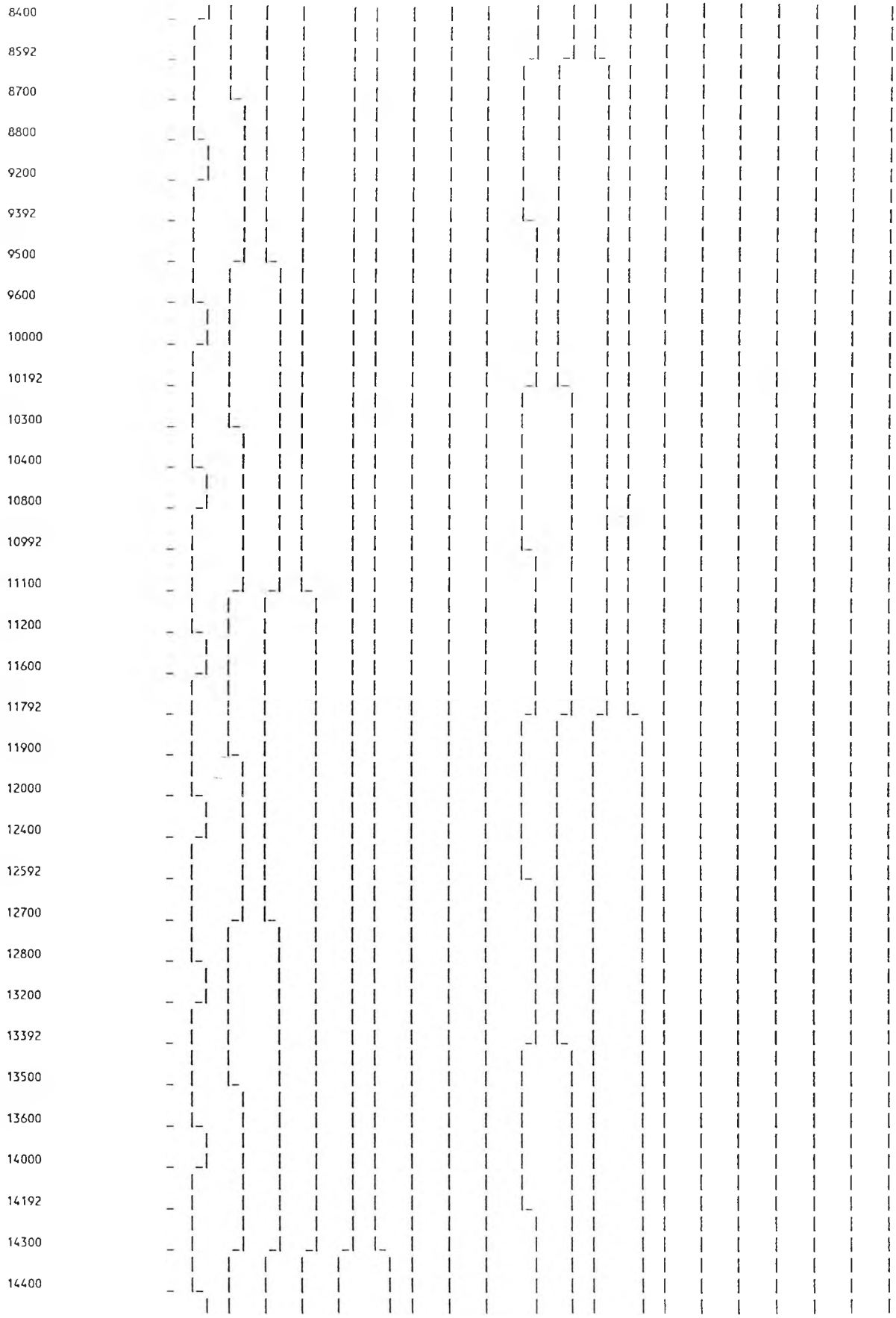


Fig. 5.14 Sysem HILO simulation results.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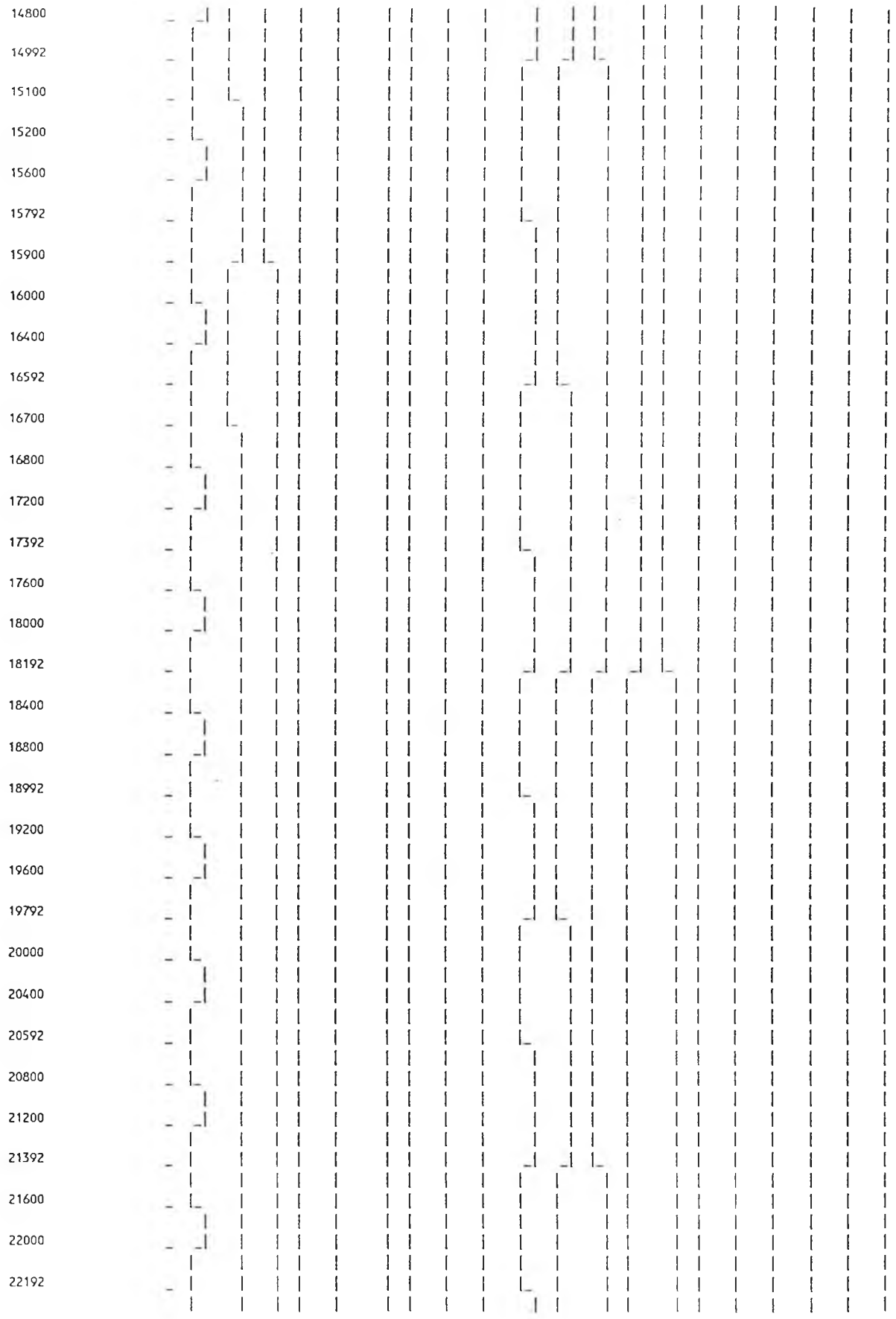
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5.6 Summary

In this chapter the design and analysis of the recorder unit was considered in detail. The recorder unit consists of two main subunits namely the optical receiver and the RAM bank and its associated control circuit. The emphasis of the chapter was on the control circuit of the RAMs which ensure the correct operation of the recorder unit. The simulation results of the recorder unit circuit confirmed the validity of the circuit design. The control circuit provides the features of programmable trigger threshold level and pretrigger data length. The control circuit also communicates with the computer during the data retrieval process from the RAM bank. In the next chapter the practical aspects of the DOCTR system are considered. These include the design of the screening box for the capture unit, the construction of the recorder unit circuit board capable of high speed operation and the interface unit between the recorder unit and a PC.

CHAPTER 6

PRACTICAL REALISATION OF THE DOCTR SYSTEM

6.1 Introduction

In this chapter the construction details of the digitising capture unit and the recorder unit are discussed and the test procedures concerning the screening efficiency for the capture unit shield considered.

This chapter will discuss the subjects of the ADC and the optical transmitters in relation to the capture unit shield. It will also discuss the regulation, monitoring and remote control of the capture unit battery supply and present the designs for the corresponding circuits. The designs of the capture unit shield and of the required cutoff

waveguides are also presented. The cutoff waveguides allow the fibre optic cables access to inside the shield while attenuating any interference signal to negligible level.

The design and construction aspects of the recorder unit board are discussed in relation to the speed of operation of the units.

Also in this chapter, details of the interface between the recorder unit and a standard computer (IBM PC or compatible) will be presented covering both the hardware required and the software developed for the interface. The PC interrogates the recording unit continuously, retrieves the stored data from the RAM bank when the required signal is captured and programmes the control circuits, if necessary, before re-arming the recording unit for further recording. Software is developed that allows the recorder unit to communicate with the PC and also enables the user to program the recorder unit for the settings to be used during data capture in the unit. The procedures for testing the efficiency of the screening box are discussed in the last section of this chapter.

6.2 The Digitising Capture Unit

The digitising capture unit is one of the two separate parts which make up the DOCTR system; the other one being the recorder unit. In contrast to the recorder unit, which is operated in interference-free area, the capture unit operates in the hostile environment where the strong electromagnetic interference could affect the operational performance of the unit, unless special measures are taken. The function of the capture unit, is to digitise the random transient that is generated within the hostile environments and launch the corresponding data into the optical link connecting it to the recording unit. In doing this it must not perturb the measurement point, while at the same time it must be physically close to the circuit concerned. This means that the physical dimensions of the capture unit are critical. A compact size of the capture unit box may reduce the disturbance effect on the measurement point and also make it accessible to parts of the circuit where space is limited.

In addition to these requirements, the electronic circuits which make up the core of the capture unit must be protected from the electrical interference to ensure the correct operation of the unit.

The capture unit is shielded by the its box and has its own battery supply within the box. The capture unit consists of an Analogue-to-Digital Converter, optical transmitters and associated voltage regulating circuits. The optical transmitters convert the digital output of the ADC to light signals to be launched into the optical fibres. The fibre optic cables reach inside the shield of the capture unit via circular cutoff waveguides fitted in the shield, designed to attenuate any outside interference to negligible levels inside it.

6.3 The ADC

The converter used in this application is Plessey's flash ADC (the SP97508), capable of samplings rates up to 110 MS/s at 8 bit resolution. This ADC was selected since it showed superior Effective Bits (EB) performance over those manufactured by other manufacturers in tests measuring the EB resolution of different ADC's at a specific sampling rate (100 MS/s) for a range of analogue input frequencies (1-50 MHz) [Mapleston, 1989].

The analogue input to the ADC is applied via a 50-Ohm SMC-type coaxial line connector mounted on the board. Another type of input required for the ADC is the clock signal which is also applied to the board via an SMC connector. The clock signal source is a crystal oscillator which is packaged in standard 14 pin DIL format. The clock circuit is placed on the optical transmitter board and drives the ADC board through a 50 Ohm coaxial cable. The digital outputs of the ADC are latched into an octal ECL-compatible buffer (Plessey's SP9210) which is capable of driving 50 Ohm lines. The buffer outputs drive the optical transmitters of the optical link. In addition, the ADC board allocates a clock output which is used to drive a separate optical channel. This clock signal is needed to synchronise and write the digital data in the

high speed RAMs at the recorder unit. The circuit diagram and layouts of the ADC board are given in Appendix D. The ADC board requires two external voltage supplies; -5.2 Volts for the digital section of the circuit and +12 Volts for the analogue electronics at the front of the ADC chip. The outputs of the buffer (ADC) and the clock output are connected to the optical transmitter inputs by equal lengths of 50 Ohm coaxial cable (this is a parallel link and path differences between the individual lines must be ideally zero). Line terminations are provided at the transmitter inputs.

6.4 The optical Transmitters

The optical transmitters are driven by the digital output of the ADC via 50-Ohm coaxial cables. The transmitters may be powered to standard ECL levels (V_{cc}=0, V_{ee}=-5.2V) or to Pseudo-ECL levels (V_{cc}=+5V, V_{ee}=0). For convenience of interfacing between the ADC output and the inputs of the transmitters, the latter are operated in standard ECL mode. The optical receiver's noise rejection performance is at its best when it is powered to pseudo-ECL levels and in the Recorder unit the optical receivers are operated in this mode. However, because of the electrical isolation between the transmitter and receivers, the performance to the optical link is not affected by the different electrical power modes in which the transmitter and receiver are operated.

The width of the ADC board dictates that of the capture unit box, and therefore the transmitters are placed on two parallel circuit boards which can be fitted within the width of the box. Nine optical transmitter modules are used in the optical link connecting the capture unit and the recorder unit. One of the transmitter boards therefore accommodates five modules and the other four.

The external clock oscillator required to drive the ADC is placed in the vacant space on one of the transmitter boards. The clock comes in 14 pin DIL package (similar to that of the transmitter modules) and drives the ADC via a 50-Ohm coaxial line.

6.5 The Battery Supply

The subunits of the capture unit are powered by battery cells accommodated within the capture unit shield. The use of a battery-based supply for the capture unit eliminates the need for a special precaution against interference on power lines. At the same time the supply of the unit will not be dependent on a supply system which could be vulnerable to earth current loops, voltage fluctuations etc.

The ADC requires two voltage supplies; +12V and -5.2V and the optical transmitter operates with a -5.0V supply. The latter supply should be capable of delivering a current of about 1400 mA.

Lead Acid cells are used to provide the current and voltage supplies required. These cells have a nominal output of 2V and are available in different capacities.

For the optical transmitter supply three 5Ah cells are used in series to give a total output voltage of 6V. For the ADC three 2.5Ah cells are used in series for the -5.2 V supply and a single 12V 0.8Ah battery is used to provide for the positive voltage. The batteries will supply power for more than three hours under these current consumption conditions.

The output voltage of three in-series cells is a maximum of 6.6V when fully charged. This output is regulated to the required level and also monitored for low voltage state. The 12V battery output does not need to be regulated since it is the same as the nominal voltage required, but it is monitored for low voltage state. In Appendix H the voltage regulation circuits are presented taking into account the operation voltage range of each of the subunits in the capture unit.

6.6 The Capture Unit Shield

The main function of the capture unit shield is to protect the sensitive electronic circuits and devices against EM interference. The shield houses all the electronic circuits of the capture unit as well as the batteries which power these circuits. The shield has been made in two separate sections; the circuit enclosure and the battery

enclosure or box. The two enclosures are attached to each other by a 9 pin screened D connector to connect the battery supplies to the circuits. When the batteries are discharged this is indicated by voltage level monitoring circuits. The battery box is then simply replaced by another one with fully charged batteries without the need to disturb the circuits or the circuit enclosure. The design of the circuit and battery boxes is discussed in the following sub-sections.

6.6.1 The Circuit Enclosure

The circuit enclosure is designed to fit the ADC circuit board as well as the circuit board for the optical transmitters. These two boards are fitted on to the demountable carrier which slides in guides within the circuit enclosure. The ADC board edge connector is fitted to the top of the carrier and the outputs of the A/D convertor are connected to the optical drivers' input through 50-Ohm RG174 A/U cables, all of equal lengths. The optical transmitters are placed on two separate (transmitter) boards and these boards are placed on both sides of the carrier. The carrier, and therefore the whole unit, can be lifted upwards to allow the connection / disconnection of the optical fibre cables. To facilitate the connection of the fibre optic cable to the transmitters while at the same time preventing any interference to leak through to the circuit, cut-off waveguides are mounted on the circuit enclosure. The 'ST' fibre optic cable connectors are small enough to pass through the cut-off waveguides.

The battery supplies regulator board is housed at the end of the circuit enclosure. The Red low voltage indicator LED's are mounted on the end of the circuit enclosure and the Power 'ON' Green LED on the adjacent side. The photodetector of the fibre optic remote switching system is placed on the corner of the circuit enclosure. A polymer fibre optic cable is used for the remote supply switching system as opposed to the silica-based cables used to transmit the high speed data.

The access to the enclosure is through a cover which is held to the top of the main box. The resulting L-shape circuit enclosure is shown in figure 6.1 with the battery enclosure completing the near rectangular unit shape.

6.6.2 The Battery Enclosure

The battery enclosure accommodates the battery cells required for the supply of the circuits of the capture unit.

The batteries used are :

Three Cyclon 2V, 5Ah lead acid battery 35.5(d)x61(h)

Three Cyclon 2V, 2.5Ah lead acid battery 46(d)x72.5(h)

One Yuasa 12V, 0.8Ah lead acid battery 95x61x23 mm

One corner of the battery box is shaped to allow the fibre optic connection for remote battery switching.

A 9-way screened D connector is used to join the battery box to the circuit enclosure.

The circuit and battery enclosures are made of 0.6 mm copper. Checks on the skin depth corresponding to the operating frequencies and the frequency corresponding to a skin depth of 0.6 mm (thickness of the screening enclosure copper) are given in Appendix E.

The skin depth equal to the copper sheet thickness of 0.6 mm corresponds to a frequency of 12 kHz.

6.6.3 The EMC Protection of the Digitising Capture Unit By the Cut-off Waveguide Technique

The main function of the enclosure is to shield the vulnerable electronic circuits of the capture unit from EM interference. Interfering signals could affect the performance of the electronic devices via the supply leads to them. In order to prevent this, an isolated

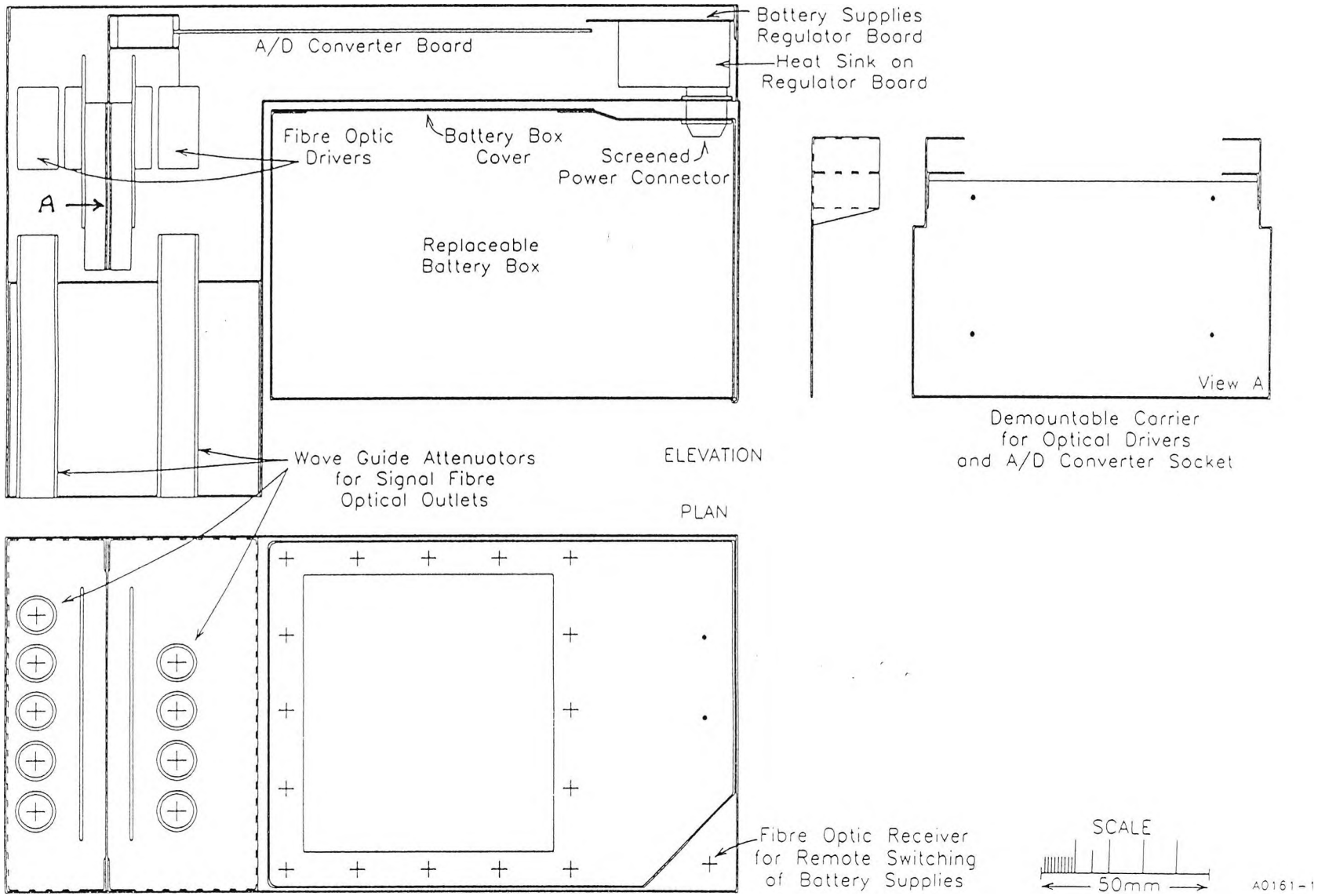

Fig. 6.1 Outline of Screening Box Showing Main Features.

battery power supply is used to power the capture unit and these cells are also accommodated inside the capture shield. But complete isolation of the capture unit is not possible since it is to be optically linked to the recorder unit. Although the fibre-optic cable is immune from EM interference, the holes through which these cables access the optical transmitters inside the capture shield leaves the capture unit vulnerable to interference. Cut-off waveguides are therefore mounted on the capture shield to allow the fibre-optic cables access to the inside of the shield while attenuating any outside interference to a negligible level inside the shield. The determination of the properties of the wave guide is presented in Appendix F.

As can be seen from the Appendix, the minimum attenuation achieved by using an 8 cm long circular waveguide of 1 cm diameter is 256 dB. For example, a 2 MV signal at the output of the capture unit shield would be reduced to a signal of the order of a μV. This waveguide therefore provides adequate protection for the capture unit by attenuating the interfering signal to an insignificant level inside the shield. The level of attenuation usually achieved by a screened room is about 100 dB.

6.7 The Recorder Unit

The physical arrangement of the different components making up the circuit with respect to each other becomes significant in very high speed circuits. At high speeds signal propagation through lines, propagation delay through the components of the circuit and their rise and fall times are comparable to the periodic times of the signal. It is of paramount importance to take these factors into account at the circuit designs stage as well as when the component layout of the circuit is being studied; the situation becomes even more critical when we have a high speed parallel system, in which another factor is intrinsically created, namely the path difference between the individual channels of the parallel route. In the design stage of the recorder circuit, arrangements have been made to take into account factors such as these to ensure the correct operation of the circuit at high speeds.

The first problem encountered in high speed circuits is waveform distortion due to line reflections . At low and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, improperly terminated lines can result in reflections. The solution is to terminate each signal line with its characteristic impedance. There are two methods of matching a transmission line; these are series-termination and parallel-termination. Depending on the application, one method may be preferred to the other.

The propagation of high speed, steep-edged signals through lines leads to the concept of crosstalk between lines [Hart, 1988] which has to be taken into account in circuit layout and board fabrication. As well as being dependent upon the magnitude of the signals, the amount of crosstalk or coupling between lines is also dependent on the direction of signal propagation as well as the geometry of the transmission lines through which the signals propagate. The forward and backward crosstalk depend also upon how far the transmission lines run parallel to each other and at what distance apart [Sugita et al, 1981; Kozuch, 1987].

Therefore before the final circuit layout is worked out, the circuit board technology suitable for the speed and density of the circuit must be established. For the recorder unit, the Multiwire circuit board technology was chosen to be suitable for the reasons given below.

The address and input data lines driving the RAMs operate at high speed (100 MHz) during the Write mode of the RAMs. Because of the size and the package of the RAMs, these lines have to run in parallel at 0.05" apart. At such proximity it is important to examine cross talk between these lines.

Multiwire technology permits such lines to run in parallel at 0.05" apart with tolerable coupling. Another requirement for the RAM bank circuit is the accurate and uniform characteristic impedance for the transmission lines. This can be achieved by multiwire, as opposed to etched tracks used by the multilayer technique; circular wires of

constant diameter (4 μm) are used in multiwire technology to give constant characteristic impedance (Z_0) and low cross talk [Botte et al, 1989].

Having established the circuit board technology to be used we now proceed with the final circuit layout for the recorder unit. Layout priority is given to those components or tracks which operate at high speed. The components which operate at high speed (during write mode) are the optical receivers, the RAMs, the address generating and data monitoring circuits, the latches, the comparators and the clock distributing gates. It is important that the path difference between the eight parallel data lines starting from the outputs of the optical receivers to the data inputs of the RAMs are kept to a minimum to avoid any errors during recording. The clock signal from the ninth optical channel is used to clock the RAMs and the latches as well as the address generating and data monitoring . In a similar manner, the outputs of the address circuits are parallel paths and the path difference between the individual lines from the output of the circuit to the address inputs of the RAMs must be minimal to ensure that the correct address data is set up at the RAM inputs. On the basis of such criteria the circuit layout for the recorder unit has been designed as shown in figure 6.2 Fig 6.2(a) shows the complete layout arrangement for the recorder unit circuit board whereas Fig 6.2(b) and (c) show the signal tracks on the component and solder sides of the circuit board.

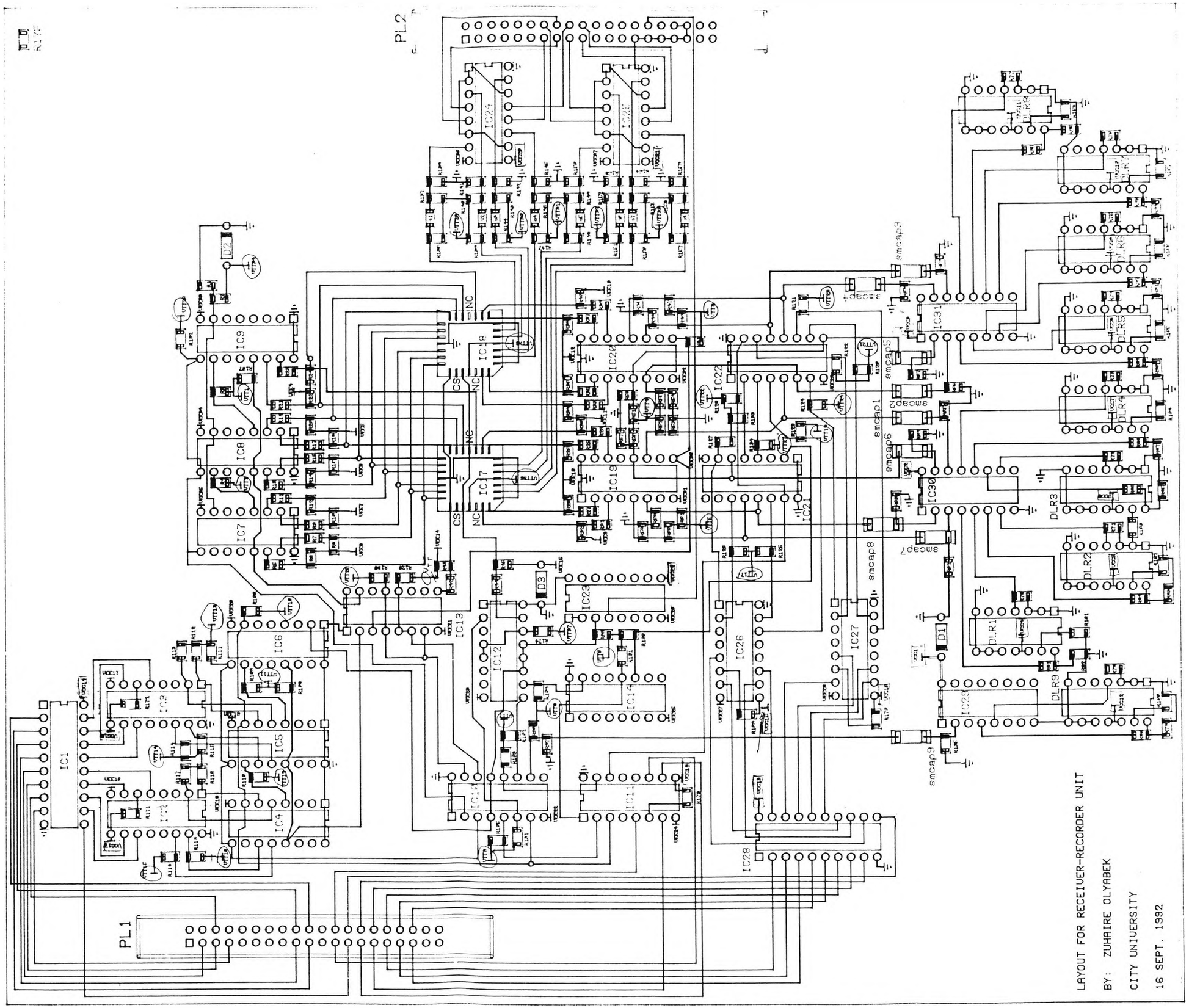

Fig 6.2(a) Layout of recorder unit circuit board

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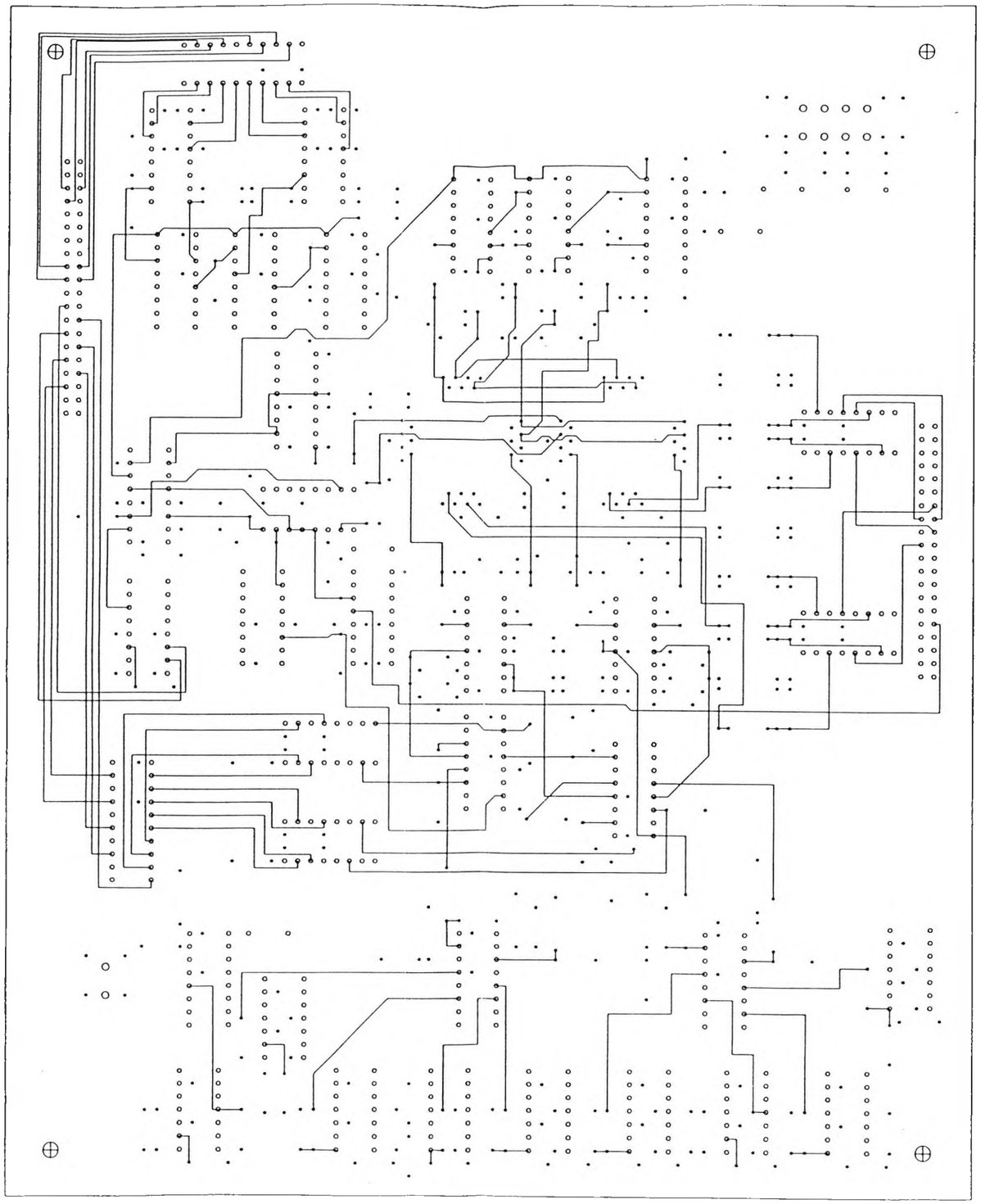
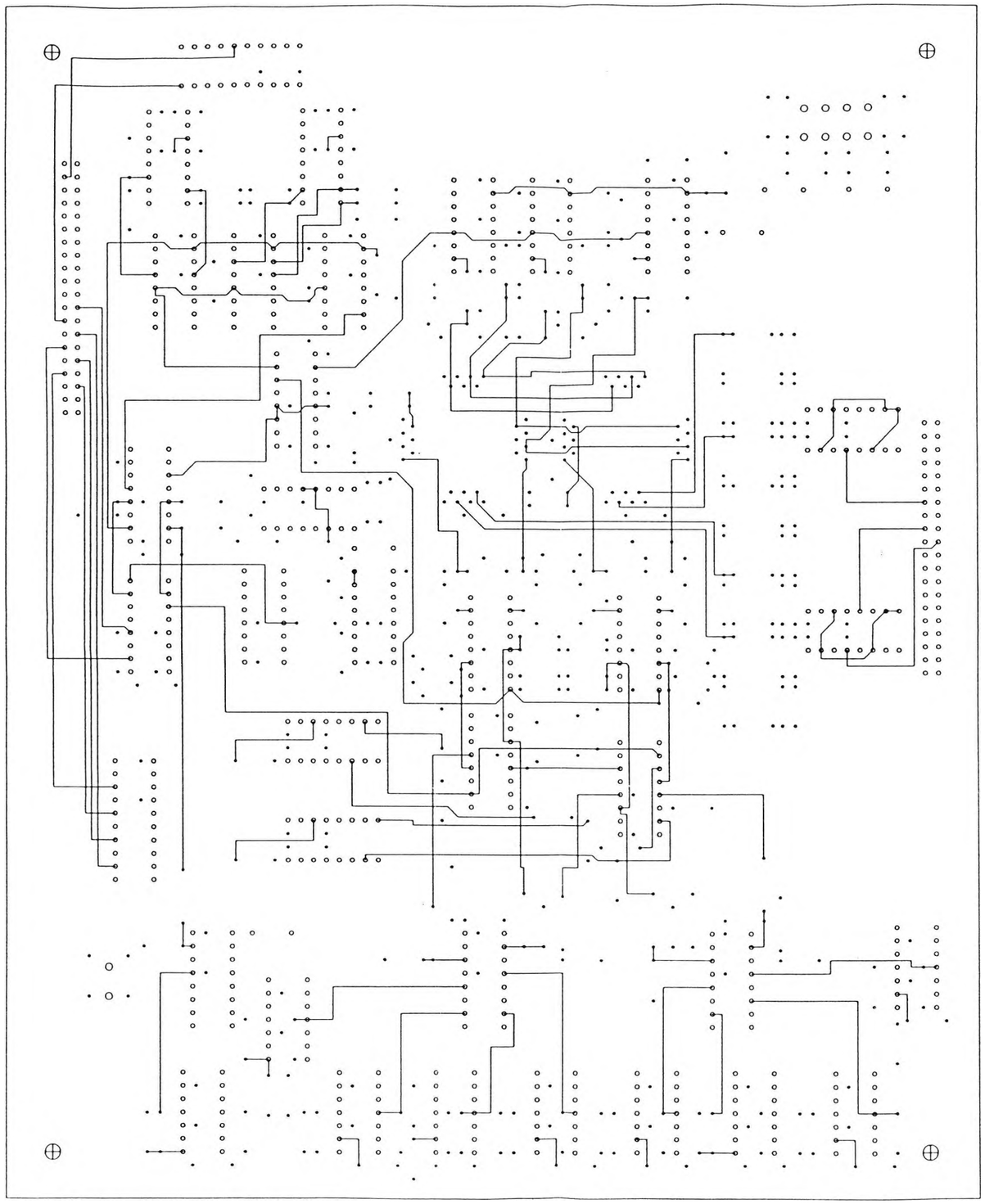


6.2(b) COMPONENT SIDE WIRING

ISSUE	A					EXACTA	CIRCUITS LIMITED SELKIRK & GALASHIELS SCOTLAND
DATE	4.5.93						
INITIALS	GM						
DRAWN	SCALE	DESCRIPTION					DRAWING NUMBER
GM	2:1	CITY UNIVERSITY , LONDON RECEIVER-RECORDER UNIT					N15127-2

CAD GENERATED DRAWING - DO NOT ALTER MANUALLY



6.2(c) SOLDER SIDE WIRING

ISSUE	A					EXACTA	CIRCUITS LIMITED SELKIRK & GALASHIELS SCOTLAND
DATE	4.5.93						
INITIALS	GM						
DRAWN	SCALE	DESCRIPTION					DRAWING NUMBER
GM	2:1	CITY UNIVERSITY . LONDON RECEIVER-RECORDER UNIT					N15127-7

6.8 The Recorder / PC Interface.

The Recorder/PC interface circuit is the hardware required to establish a communication link between the Recorder Unit and the Personal Computer. A computer programme was written to enable the PC to control and monitor the state of the recorder unit. Through the PC, the recorder settings may be chosen as required before re-arming the recorder unit. The hardware and software for the interface are presented in the following sections.

6.8.1 The Hardware

The interface board used is an industry standard digital I/O which can be programmed to have all the 48 lines to be operated as input, output or a combination of both. The 48 lines of the PC14AT are organised into six ports. The PC14AT uses two 82C55 PPI's (Programmable Peripheral Interface) each of which provide 24 I/O lines. These lines are divided into three 8 bit ports A, B and C. A different address is assigned to each one of the ports and by programming the control register, the mode of operation of each port is established. The function of the ports is defined by writing an 8 bit control word to the control register [Amplicon, 1990].

6.8.2 The Software

The functions of the software are to

* programme the interface board;
* programme the trigger threshold level
* programme the number of pretrigger samples;
* monitor the 'RAM full' flag;
* retrieve the data from the RAM unit;
* re-arm the recording unit.

The software is written in Microsoft's GW Basic programming language.

The software programmes the interface board's ports such that three ports are set as input ports and the other three as output ports. The data for the number of pretrigger samples and the trigger threshold level are set at ports A and B of the output ports respectively. The command lines to the control circuit of the recording unit use port C of the output ports.

Port A of the input ports is used to read the data from the RAMs while port B of the input ports is used by the software to monitor the status of the flag output of the control circuit of the recording unit.

The software written prompts the user for the pre-trigger sample and trigger threshold level and re-arms the recording unit once the user is ready to proceed with the recording. The data for the pre-trigger samples and trigger threshold level are programmed into separate output ports of the interface board. The software continuously monitors the status flag and when the recorder unit indicates the completion of a recording, the software takes over the control of the recorder unit to retrieve the stored data. Before re-arming the recording unit the software prompts the user should new "trigger" settings be required for the next record.

The software is listed in Appendix G.

6.9 Summary

The construction details of the digitising capture unit and the digital recorder unit have been presented in this chapter. The design of the screening box for capture unit was also discussed.

In the construction process of the circuit board for the recorder unit, the effect of cross talk between adjacent tracks carrying high speed signals was taken into account.

The hardware and the software of the interface unit between the recorder unit and the computer were also presented.

In the next chapter, the performance of all the units comprising the Digital Optically-Coupled Transient Recorder (DOCTR) system will be evaluated as well as the overall performance of the DOCTR system. In this process the hardware interface, between the DOCTR system and the computer, as well as the software specifically written for this interface will be tested.

The tests for the screening of the capture unit will also be presented.

CHAPTER 7

TESTING & EVALUATION OF SYSTEM PERFORMANCE

7.1 Introduction

In this chapter the various tests carried out on the Digital Optically Coupled Transient Recorder (DOCTR) system are discussed and the test results presented. In the run up to the tests on the complete DOCTR system, tests were first carried out on the different units of the DOCTR system to evaluate their performance. From the functional point of view, the DOCTR system may be divided in three main units which are the digitisation unit i.e. the Analogue-to-Digital Converter (ADC), the Fibre Optic Link (FOL) and the Recorder unit.

The tests carried out during this work were arranged in two stages; in the first stage, the performance of the ADC-FOL units alone was evaluated. This was to show that the ADC-FOL system operated correctly. In the second stage, the Recorder unit was tested alongside the ADC-FOL units, and the output data of the Recorder unit was analysed with reference to the input of the ADC-FOL-Recorder unit. This arrangement is that of the complete DOCTR system.

In each stage, the performance of the system under test was investigated for sinusoidal and chopped-impulse input signals.

During the first stage of tests (ADC-FOL only, without the Recorder unit), in order to monitor the output of the FOL unit on an oscilloscope or a spectrum analyser, a Digital-to-Analogue Converter (DAC) was used to display the FOL unit output. The input of the DAC was driven by the digital output of the FOL unit. Figure 7.1 shows this arrangement where the output of the DAC is monitored on an oscilloscope.

In addition to the time domain tests, the performance of the ADC-FOL units was also investigated in the frequency domain by analysing the frequency spectrum of the output of the ADC-FOL-DAC.

In the following sections the tests carried out on the ADC-FOL-DAC system are discussed. The sinusoid tests are first considered and the test results presented. This is followed by the chopped-impulse tests. The test results for the chopped impulses as input signals to the ADC-FOL-DAC system are then presented and discussed.

The next section covers similar test procedures for the complete DOCTR system which is the ADC-FOL-Recorder unit. Figure 7.2 shows this arrangement where the Recorder unit and the personal computer (PC) replace the DAC and the oscilloscope of Fig. 7.1. The test results obtained in this stage are presented and analysed.

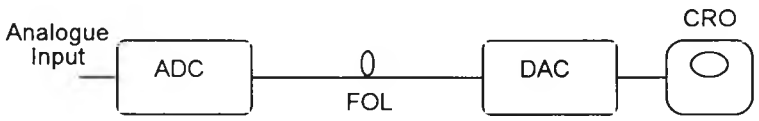


Fig. 7.1 The ADC-FOL-DAC system with the DAC output monitored on the CRO

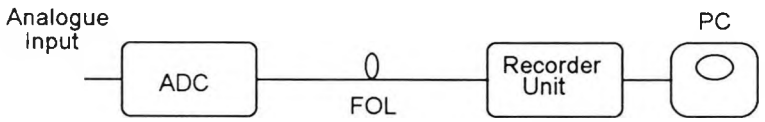


Fig. 7.2 The ADC-FOL-Recorder Unit making the complete DOCTR system. The Recorder Unit is interfaced to a PC so that the data may be retrieved and analysed by the PC

7.2 Performance Measurement of the ADC-FOL-DAC

In this stage of the investigation, the objective of the tests is to evaluate the performance of the ADC and the FOL units and obtain satisfactory results for the operation of the ADC-FOL system. To enable this measurement, a Digital-to-Analogue Converter (DAC) is used as a diagnostic tool to convert the digital data at the output of the FOL unit to analogue form to be monitored on an oscilloscope.

In such a method, in addition to the sources of error due to the ADC, the DAC also contributes to the noise of the overall system. It is therefore important to take into account the noise contribution of the DAC when the performance of the ADC is evaluated. The noise contribution or distortion of the DAC could be made insignificant compared to that of the ADC by using a very low distortion DAC such as the Tektronix DAC10 [Tektronix, 1993]. This has a linearity error of ± 0.01 LSB (Least Significant Bit) as opposed to the linearity error of the DAC used here which is ± 0.5 LSB [Plessey, 1988].

With a sinusoidal signal driving the input of the ADC, the output of the ADC-FOL-DAC system is given in Fig. 7.3. In this figure the upper trace is the DAC output and the lower trace is the input to the ADC. By comparing the DAC output to the input of the ADC, it can be seen that faithful reproduction of the input has been achieved after transmitting the digitised signal through the optical link. An apparent phase-shift can be seen between the output and the input, which is mainly due to the propagation delay through the FOL unit. The shift is 0.4 divisions which is (0.4×0.5μs) 0.2μs. The FOL unit uses 40 meter fibre optic cables and as the speed of light through the glass is 1 ns/20 cm [Kaye and Laby, 1959], the total travel time through the cable is 200 ns which is the shift seen between the input and the output. The DAC output is larger than the ADC input by a factor of 1.16. As mentioned earlier, the DAC is used only as a maintenance/development tool.

In this way, the optical link was successfully tested as a complete entity .

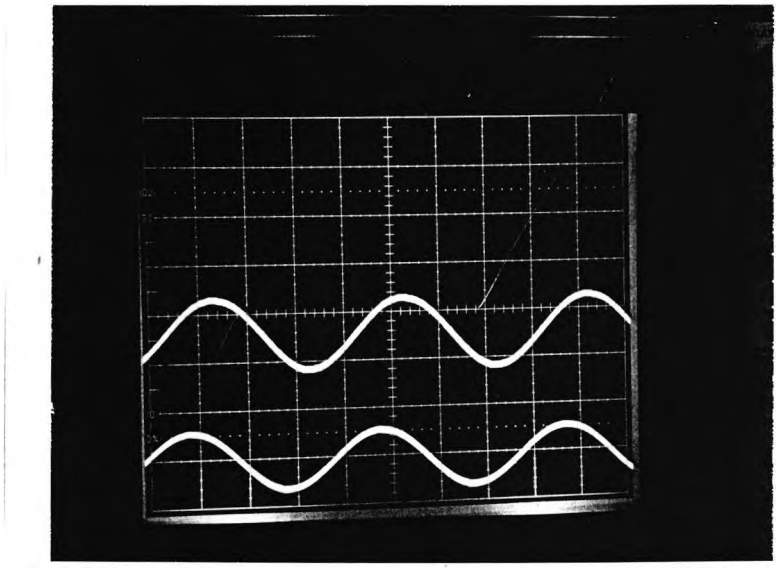


Fig. 7.3 Input (lower trace) and output (upper trace) of the ADC-FOL-DAC system. The scale for the horizontal and vertical axes are 0.5 μs/div and 0.2 V/div respectively.

Prior to using the optical link in this test, individual channels of the FOL unit were tested for their high speed performance (100 MHz). The FOL unit consists of nine channels; eight for the sample digits and one for the clock. Each channel consists of an optical transmitter, a fibre optic cable and an optical receiver. Because of the parallel nature of the optical link and its speed of operation, it is important that the path difference between the individual channels is insignificant compared to the period of the sampling clock (10 ns). The fibre optic cables were ordered to have close tolerance and a series of measurements were made to check this. The optical path length of each channel was measured and it was found that the optical path difference between the channels of the link was negligible compared to the clock cycle; the maximum path difference was measured to be approximately 0.6 ns. These measurements were carried using an oscilloscope where one optical channel was used as a reference (on channel one of the 'scope) and the path differences of the other channels were measured successively with respect to the reference channel (on the second channel of the 'scope). The horizontal resolution of the scope was set to 1 ns/div with sub-divisions of 0.2 ns (in the $\times 10$ mode) and the difference between the corresponding wavefront edges of the two optical channels were visually observed.

The next phase of these tests is to investigate any signal distortion of the ADC-FOL-DAC system. This is done by spectrum analysis of the signals at both the input and the output of the ADC-FOL-DAC system.

An analogue to digital converter has an inherent quantisation error of $\pm$ 0.5 LSB. However, an ideal converter has zero linearity error. In practice, converters have a finite linearity error, and with present converters, this is usually $\pm$ 0.5 LSB. This linearity error manifests itself as an unwanted harmonic in the output spectrum.

For the purposes of investigating the linearity error, and therefore signal distortion, of the ADC-FOL-DAC, it is ideal to use input sinusoid signals which have insignificant levels of harmonics (more than 40 dB below the fundamental). Therefore during these tests attempts were made to use sinusoids with relatively low levels of harmonics.

A signal generator, the Ferrograph, was used to give sinusoidal signals with relatively low harmonics but this performance was limited to frequencies up to 10 kHz. Fig. 7.4 shows the frequency spectrum of the output of the Ferrograph signal generator which is input to the ADC-FOL-DAC. The corresponding DAC output is shown in Fig. 7.5. Fig. 7.5 shows an additional harmonic due to the ADC-FOL-DAC which is at -65 dB (relative to the 0 dB line at the top of the grid). With the fundamental being at -8 dB, the additional harmonic is at 57 dB below the fundamental.

For higher frequency input signals, the Marconi 2019A signal generator was used. The harmonics associated with the signal from this generator were too high for the purposes of this test (30 dB below fundamental). A filter was therefore used to obtain a sinusoid with much lower levels of harmonics. The filter had a low pass bandwidth of 3 MHz and a 45 dB attenuation at 5 MHz. The frequency spectrum of the filtered output of the Marconi 2019A is shown in Fig. 7.6. The output level was 500 mV peak-to-peak and its frequency 3.2 MHz. Fig. 7.6 shows the display of the spectrum analyser scanning the (input) signal from 0 to 100 MHz. Two peaks can be seen on the left of the display. The first one is the mains 50 Hz signal and the second is the input signal. The screen marker (pointing downward) is positioned at about the centre of the screen. It can be seen that no significant harmonics are present at the output of the filter within the spectrum of 100 MHz. The output of the Marconi 2019A drives the input of the ADC-FOL-DAC and the corresponding DAC output is shown in Fig. 7.7. This figure shows the harmonics obtained at the output of the ADC-FOL-DAC, the highest of which is at -73 dB. With the fundamental at -26 dB, the highest harmonic is therefore at 47 dB below the fundamental. The harmonics at the right of the screen are due to the 100 MHz sampling clock frequency.

7.3 Testing of ADC-FOL-DAC using Chopped Impulses

As well as the tests carried out using sinusoidal inputs to the ADC, chopped impulses were also used to test the performance of the ADC-FOL-DAC.

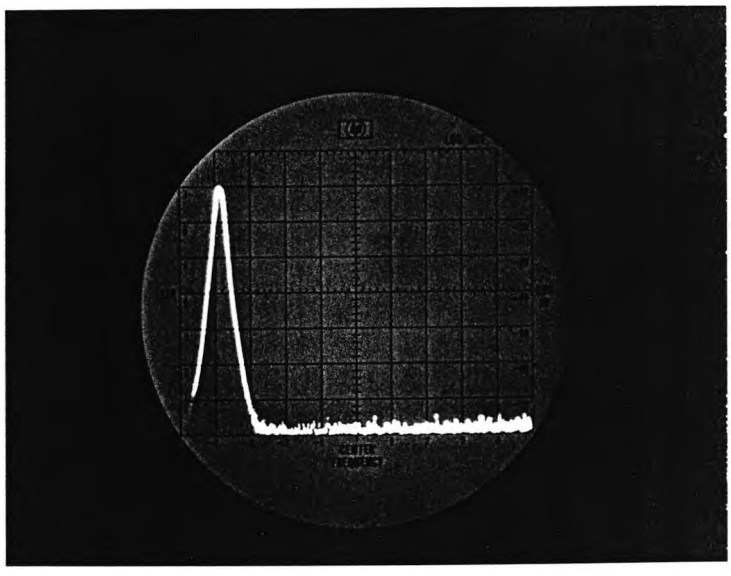


Fig. 7.4 Frequency spectrum of the output of the Ferrograph generator. The top and bottom grid lines at 0 dB and -70 dB respectively and the scale is 10 dB/div. The fundamental can be seen to be at -10 dB. Horizontal scale is 20 kHz/div.

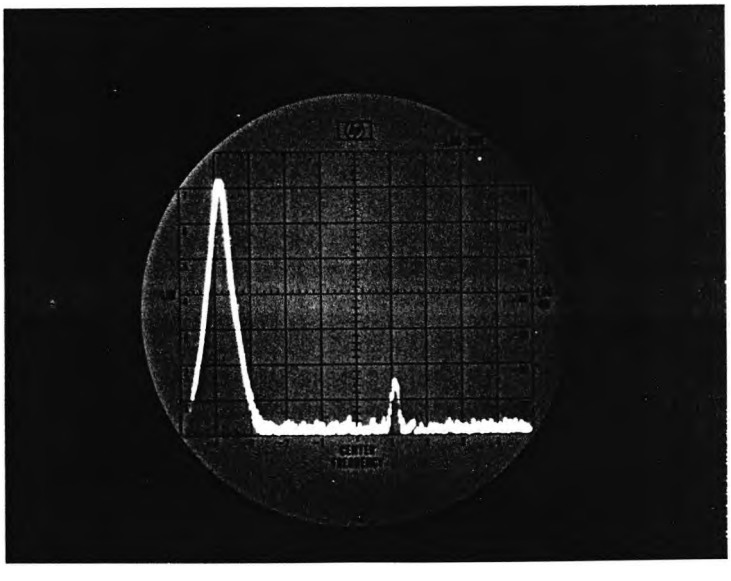


Fig. 7.5 Frequency spectrum of the output of the ADC-FOL-DAC system.

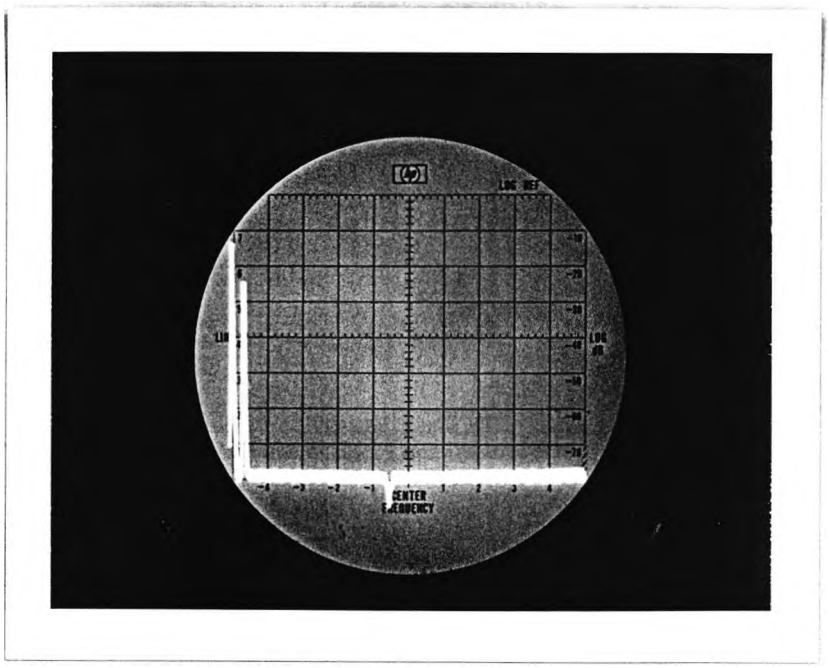


Fig. 7.6 Frequency spectrum of the filtered output of the Marconi generator over the frequency range of 0-100 MHz.

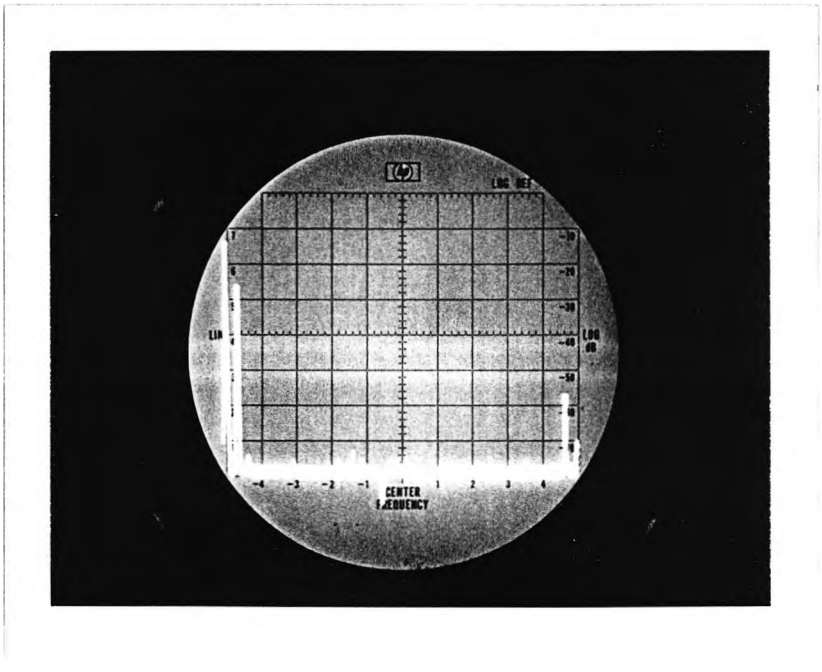


Fig. 7.7 Frequency spectrum of the output of the AC-FOL-DAC system over the frequency range of 0-100 MHz.

For this purpose a circuit was designed to generate chopped impulses repeatedly. The design of this circuit is described in Appendix I. The impulses had a rise time of 1 μs. With this circuit, the impulse wave could be chopped at any point from near its peak value to the tail of the wave and that the chop time could be determined, down to less than 100 ns. A typical output of this circuit is given in Fig. 7.8 with a chop time of 100 ns.

Fig. 7.9a shows the output of the ADC-FOL-DAC (upper trace) when driven by the pulser circuit at the ADC input (lower trace). Fig. 7.9b shows the two waveforms on a faster time base. Figs. 7.10a and 7.10b show the pulser output stored in a digital scope (Tektronix 7854). Fig. 7.10a indicates the peak value of the pulse (233 mV) and the rise time (0-100%) of the waveform (953 ns). In Fig. 7.10b the cursors are positioned on the chop applied to the waveform showing a chop time of 105 ns. Figs. 7.11 show the corresponding output of the DAC when the ADC is driven by the pulser circuit. Fig. 7.11a shows that the peak of the pulse is 284 mV and its rise time is 953 ns. Fig. 7.11b shows that the chop time is about 110 ns. These figures show that the ADC-FOL-DAC system is capable of digitisation and transmission of rapidly changing signals at the speed of 100 mega samples per second (MS/sec).

During the chopped-impulse tests, it was found that the driver circuit of the ADC chip (on the ADC board) was unstable. This was confirmed by Plessey engineers [Ikin, 1993] (the manufacturers of the ADC chip and the board) who pointed out that the ADC driver (the SL9999) is the cause of this difficulty. This instability particularly manifested itself for the chopped-impulse inputs.

When the input is a sinusoid, the problem of instability does not occur if the offset bias is adjusted correctly. However, for the impulse inputs, the adjustment for stability was extremely critical and even then only lasted for up to a minute. The effect of this instability is the 'disintegration' of the signal at the DAC output and continuous adjustment of the 'offset' potentiometer on the ADC board (RV1) was needed to ensure good output. Fig. 7.12 shows the DAC output when slightly 'disintegrated'

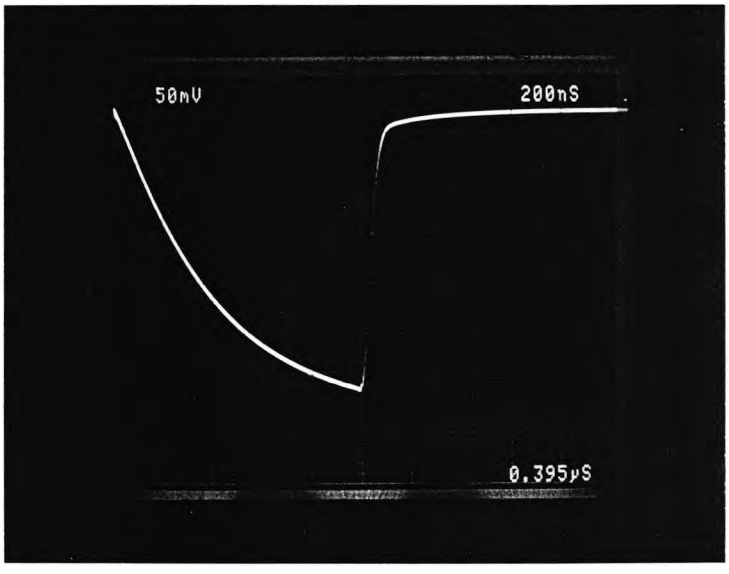


Fig. 7.8 Typical output of the chopped-impulse circuit with rise and chop times of about 1 μs and 0.1 μs respectively.

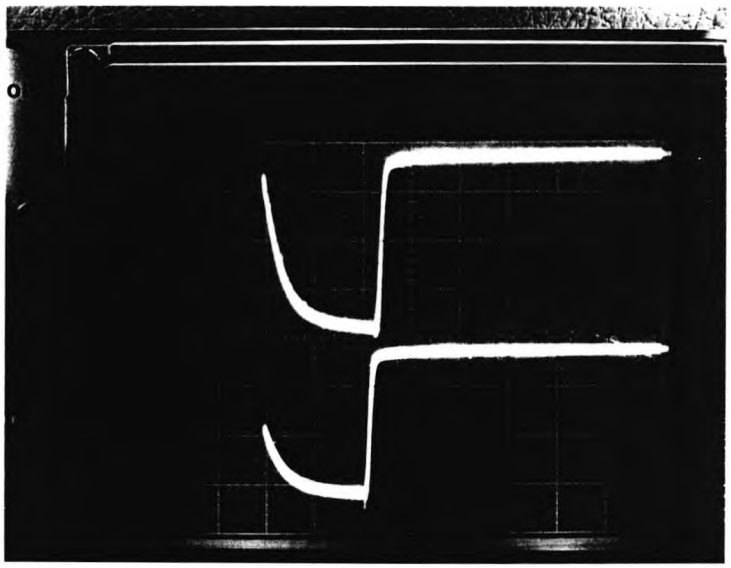


Fig. 7.9a Chopped-impulse input to the ADC (lower trace) and the corresponding output (upper trace) of the ADC-FOL-DAC. (↑ 0.1 V/div, → 1 μs/div)

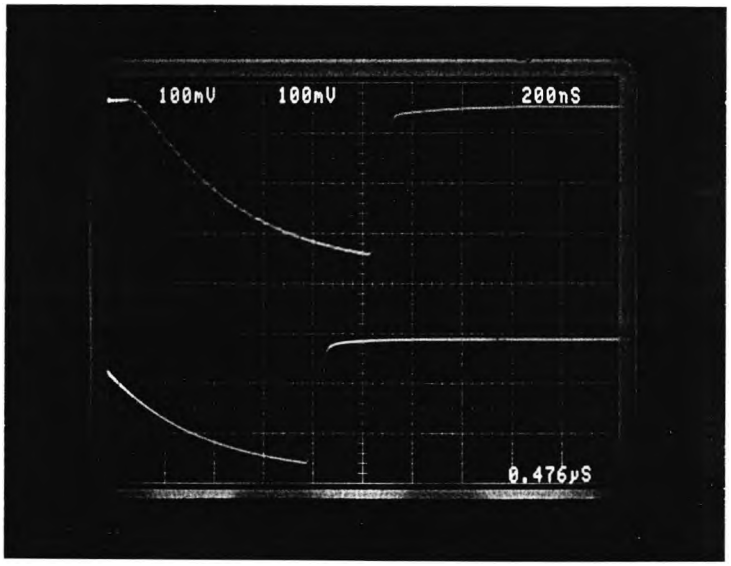


Fig. 7.9b Chopped-impulse input and output of the ADC-FOL-DAC system on a faster time scale. (200 ns/div)

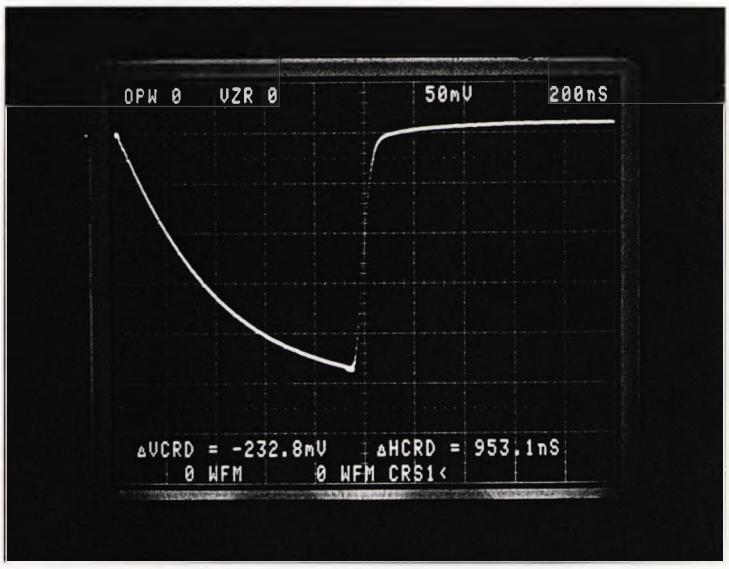


Fig. 7.10a Input to ADC; impulse wavefront of 233 mV peak and rise time of 953 ns

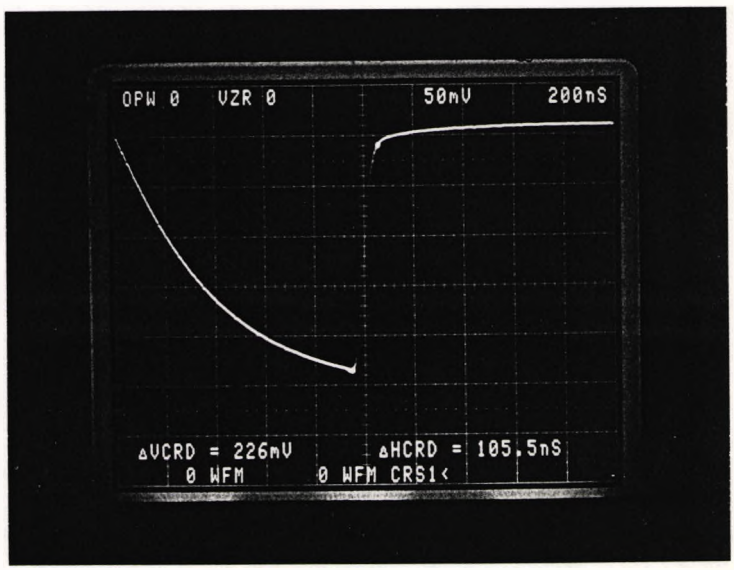


Fig. 7.10b Input to ADC; impulse chop time of 105 ns.

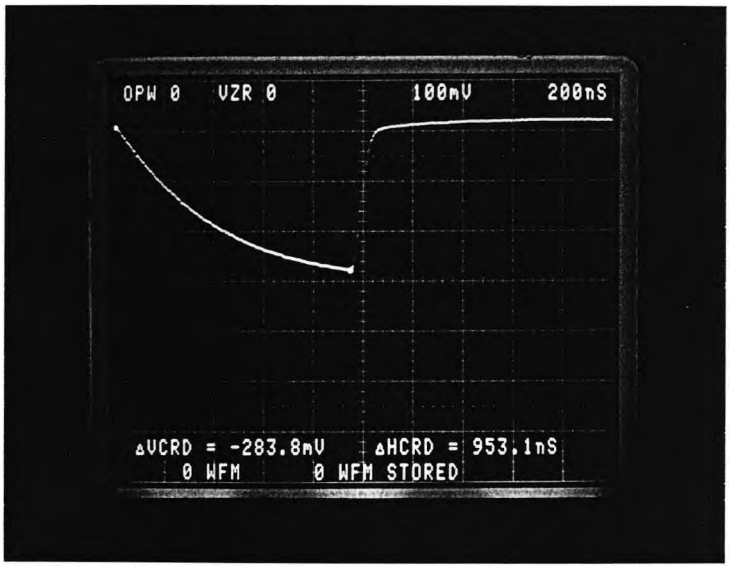


Fig. 7.11a Output of ADC-FOL-DAC; impulse wavefront of 283 mV and rise time of 953 ns.

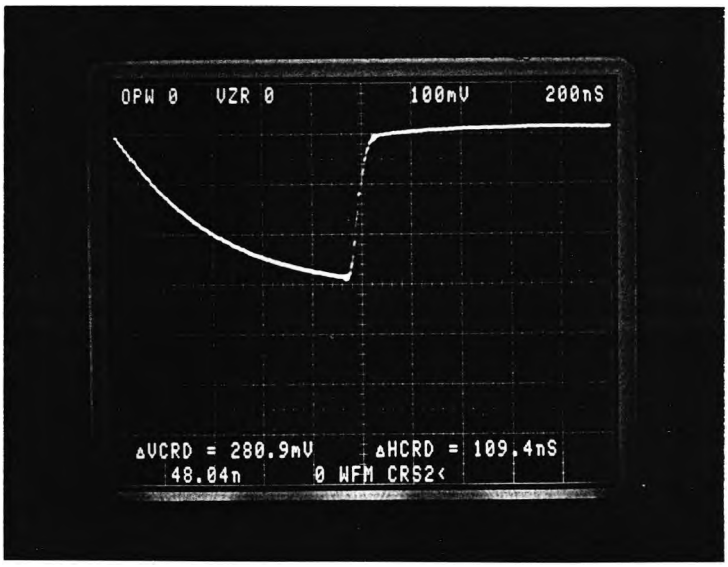


Fig. 7.11b Output of ADC-FOL-DAC; impulse chop time of 109 ns.

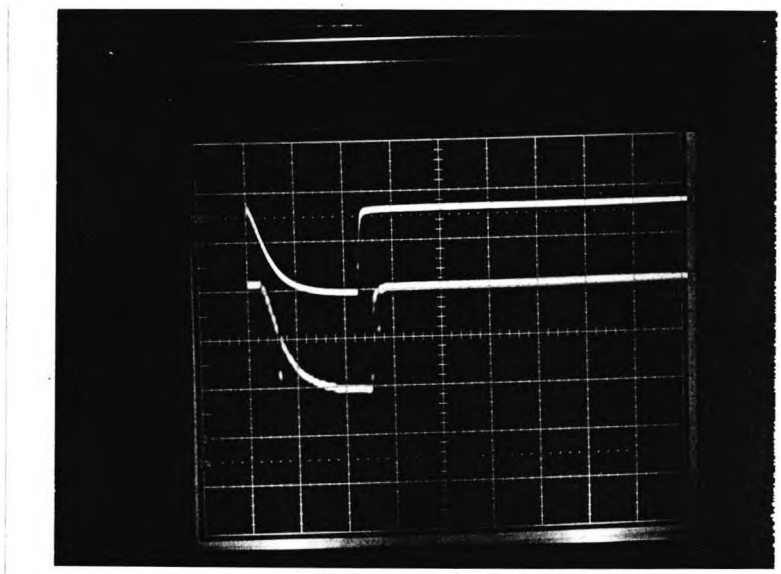


Fig. 7.12 'Disintegrated' output (lower trace) of the ADC-FOL-DAC due to ADC driver instability. Upper trace is the input to the ADC. → 1 μs/div. and ↑ 50 mV/div.

(lower trace). The upper trace is the input to the ADC board.

These tests had to be done in a manner in which the short period of stable ADC driver operation was not critical to the results, since it was not possible to spend time or money to correct this problem in this phase of the project.

7.4 Capture Unit Screening Tests

In separate tests, the performance of the screening of the capture unit as well as that of the FOL unit in the presence of HV impulses were tested using the ADC-FOL-DAC system. The capture unit consists of the ADC and the transmitter end of the FOL unit which are housed in a screening compartment. The material of the screening compartment was copper of 0.6 mm thickness. Discussion of the design and construction of the screening compartment, or shield, is presented in section 6.6 of chapter six and in Appendices E and F.

The capture unit was placed in the hall of the HV laboratory. The optical cables were led from the capture unit in the hall of the HV laboratory to the Gallery where the optical receiver/DAC were placed. The Gallery of the HV laboratory was first regarded as an electrically 'safe' area and no special precautions were taken to screen the receiving units. The screening for the Gallery (only 50 dB) was shown to be inadequate and eventually double screening was required for the receiving units.

The capture unit was subjected to a strong electromagnetic field by locating it close to HV impulse generator operating at 800 kV. The distance of the signal capture unit from the centre of the sphere gaps was 1 meter. Any interference signal within the shield of the capture unit is detected by the ADC and is transmitted through the FOL to the DAC.

The single shot output of the ADC was smaller than the inherent noise of an ideal converter (0.5 LSB, equivalent to 2 mV) that it could not be distinguished in the presence of that noise. The shield was designed to have, theoretically, a minimum

attenuation of 256 dB (Appendix F). For this level of attenuation and an interference signal of 800 kV, the signal within the shield would be very small (around 0.1 μV). Even if in practice the shield attenuation is poorer than that obtained by calculation, the resulting interference signal within it would still be relatively small. More elaborate screening measurement techniques have been reported by Malewski et al [1982].

It was therefore be concluded that the shield provides sufficient screening against EM interference for the sensitive electronic circuits. It was not possible to check the screening of the unit when subjected to a low frequency magnetic field. Using the skin depth calculation (Appendix E), the thickness of copper used for the shield corresponds to 12 kHz and therefore the shield would not adequately screen signals of lower frequencies.

7.5 Testing of the Recorder Unit.

Having successfully tested the operation of the ADC-FOL-DAC system, the aim of this second stage of the tests was to investigate the performance of the Recorder unit. The DAC was replaced by the recorder unit and the emphasis was on the Recorder unit since the ADC-FOL was proven for its integrity.

The recorder unit consists of the optical receivers, the high speed random access memories (RAMs) and the associated control circuits. The recorder unit is interfaced to a personal computer (PC) using a standard digital input/output card.

The input of the recorder unit is driven by the output of the FOL unit, while the digital output of the ADC drives the FOL unit input. The analogue input signal is digitised by the ADC, transmitted through the FOL unit before the corresponding digital data is stored in the memory of the recorder unit. The data retrieved from the recorder unit is displayed on the computer screen. This data is compared with the input to the ADC.

Two types of signals were used during the test of the recorder unit, a sinusoid and a repetitive chopped-impulse signal. In the first test of the recorder unit, the ADC was driven by a sinusoid. The ADC was clocked at a sampling rate of 100 MS/sec and during this stage of the test the input signal frequency was set to 220 kHz. This signal frequency was chosen in order to capture at least two cycles of the sinusoid in the RAM of the recorder unit. After the acquisition of a record by the DOCTR system, the reconstructed data retrieved from the RAM's of the recorder unit is shown in Fig. 7.13.

A number of "glitches" appear on the output data which are not associated with the input signal driving the ADC in the probe unit. These "glitches" are not due to the fibre optic link since the tests on the ADC-FOL-DAC proved successful. Also the incoming data at the input of the RAMs was monitored using the HP16500 logic analyser and such "glitches" were not detected.

A closer look at the position of these "glitches" and their heights reveals two points

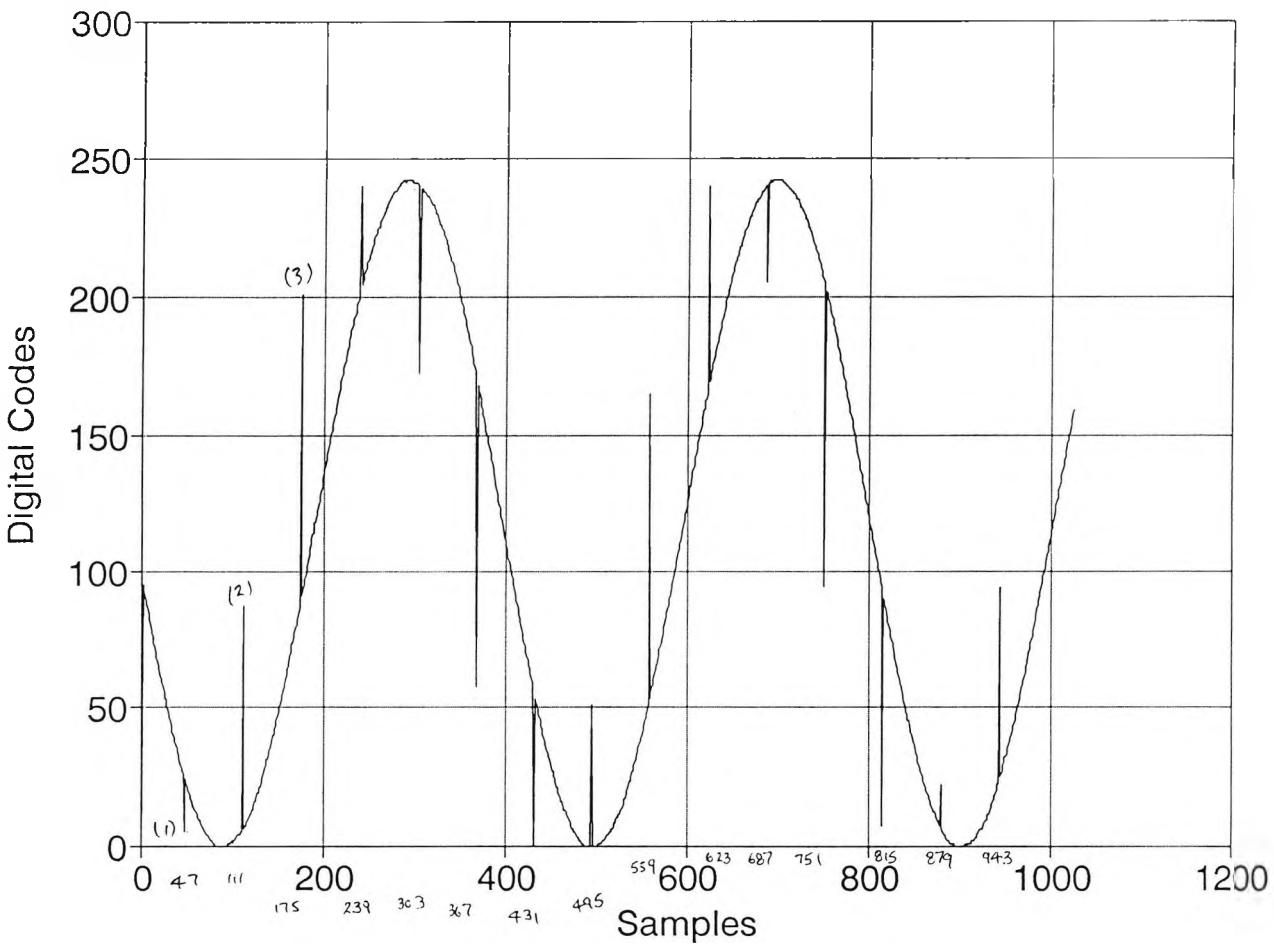


Fig. 7.13 Computer display of the acquired data retrieved from the recorder unit.

about their nature. Firstly the "glitches" are consistently spaced 64 address locations apart (on the horizontal axis) and secondly the peak of each glitch corresponds to the base of the following glitch (on the vertical axis).

In fact what has given rise to each "glitch" is that the correct data corresponding to the "glitch" has been stored at an address location 64 places earlier, and that the height or the data stored at the address location where the glitch has appeared should have been stored at 64 address locations ahead. Referring to Fig. 7.13, the data of glitch (2) (address 111) has been stored at the address location corresponding to glitch (1) (address 47) and the data of glitch (2) corresponds to the address location where glitch 3 is present (address 175) and so on.

If this problem had occurred during the writing of data in the RAMs, it could be said that the address generating circuit may be the cause of the problem. The address generating circuit provides 10 address lines (A0-A9) to the RAMs. The seventh address line, A6, corresponds to 64 (2^6). The fact that the data is displaced by 64 address locations *could mean* that A6 address line responds 'too slowly' compared with other address lines and therefore when the rising edge of the clock pulse arrives, the new state of A6 is not clocked in. A possible scenario for this phenomena is for example if the counter is counting up, say from 0, then the count after 63 is 64. But if the A6 address line is responding too slowly whereas the rest of the lines change state in time, then the count would be seen to go from 63 to 0 before reaching 65 with count 64 being 'lost'. This is outlined in binary as follows:

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Decimal Value
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	0	62
0	0	1	1	1	1	1	1	63
0	0*	0	0	0	0	0	0	0..replaces next count
0	1	0	0	0	0	0	0	64....'skipped' count
0	1	0	0	0	0	0	1	65

* not changed to '1' yet

Table 7.1 The scenario for the address count (64) being 'skipped'.

In the above table, the starred digit should have changed state from 0 to 1 as well as the changes of A_0 to A_5 . This gives rise to having count 0 after 63.

Using the HP16500 logic analyser, a series of 'state' and 'timing' analyses were therefore carried out to investigate this phenomena and identify the source of this error. The analyses were targeted on the data at the input and the output of the RAMs and also on the addressing of the RAMs during the 'write' and the 'read' modes. (For the purpose of these analyses only, because of the limited bandwidth of the logic analyser, the sampling and recording speed of the DOCTR system was changed from 100 to 10 MS/sec.)

Four categories of analysis were carried out which are discussed below:

1. Timing analysis of the address inputs of the RAMs (during 'write' mode)

While data was being recorded in the RAMs, the address lines driving the inputs of the RAMs were monitored to check for the possible timing errors using the timing analyser. No address discrepancy was present. Fig. 7.14 shows the address lines A0-A9 while changing state and there is no delay for A6 to change state. Even if there

were a relatively slower response between one address line and another, the circuit is designed so that the rising edge of the clock (RAMCLK in Fig. 7.14) arrives almost half of a clock cycle after the address lines have changed state to allow for any individual address line delays as can be seen from Fig. 7.14. Fig. 7.15 shows the same condition as Fig. 7.14 but over a wider time scale.

In general, the logic analyser samples the lines at regular intervals. In this the case address lines are sampled at intervals of 10 ns which is the shortest period for the logic analyser. In order to check if the address line A_6 is changing state between two consecutive samples, it was decided to monitor A_6 on the CRO with reference to the RAMCLK. Fig. 7.16 shows the signal on the address line A6 (lower trace) as well as the RAMCLK signal (upper trace). This figure shows that the A6 signal has been present for half a cycle when the rising edge of the RAMCLK arrives which is in agreement with the timing diagram of the logic analyser. Fig. 7.17 shows the same condition as Fig. 7.16 but on a wider time scale. Therefore these "glitches" are not caused by the incorrect operation of the address generating circuit of the recorder unit during the 'write' mode. Similar results to the record of Fig. 7.13 (sampling rate 100 MS/sec) were obtained for the sampling frequencies of 50 MS/sec and 10 MS/sec.

2. Timing analysis of the address inputs of the RAMs (during 'read' mode)

Having established that the "glitches" are not caused by the address generating circuit of the recorder unit during the writing process, it was decided to investigate the process of retrieving the data from the RAMs by the computer. It is a possibility that these "glitches" are caused during the reading of the data in the RAMs of the recorder unit by the computer and/or the input/output card.

During the reading of data from the RAMs of the recorder unit by the computer, the address generating circuit and the RAMs are clocked by the computer via the input/output card. The computer reads the contents of every address location in the RAMs and re-arms the recorder unit (if instructed by the user) for further data

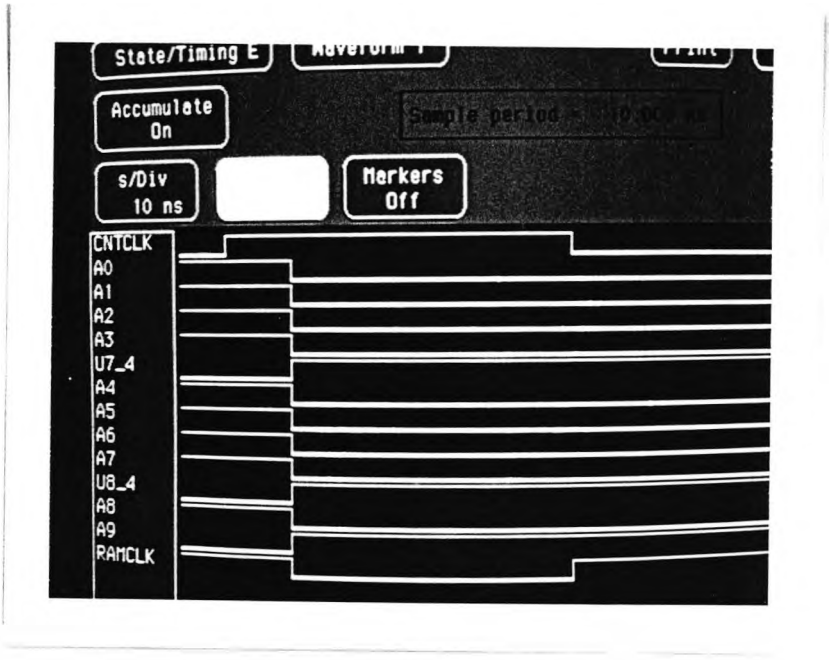


Fig. 7.14 Timing diagram of the address lines driving the RAMs while data was being recorded in the RAMs. In this instance the address lines A0-A9 are changing state from 01 1111 1111 to 10 0000 0000.

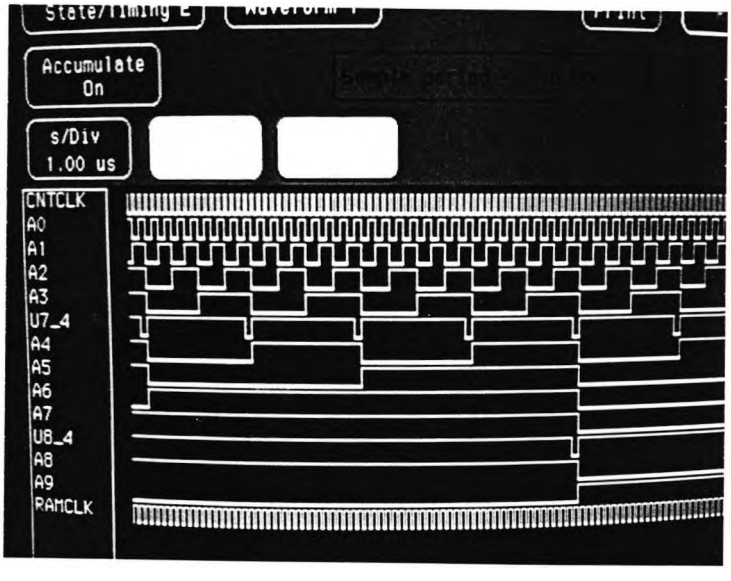


Fig. 7.15 Same as above but over a wider time scale.

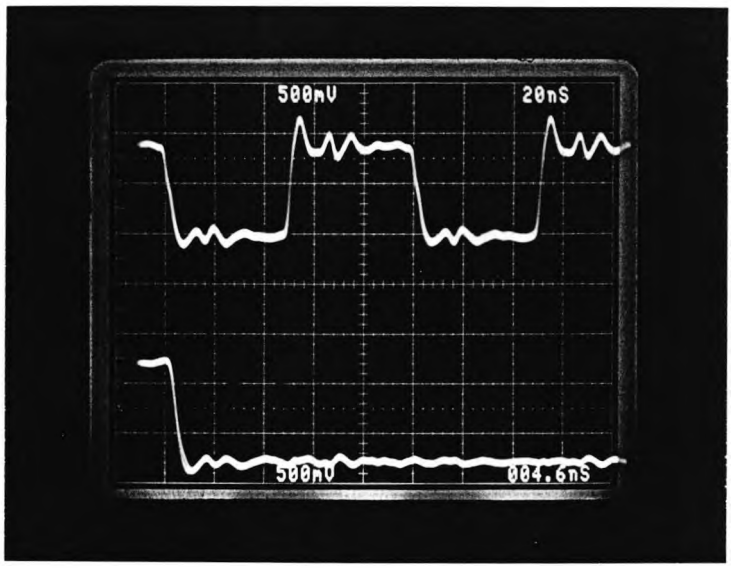


Fig. 7.16 The RAMCLK signal driving the clock input of the RAMs (upper trace) and the signal on the address line A6, during the 'write' mode, monitored on the oscilloscope (the Tek 7854). This shows that the A6 signal is stabilised half of a clock cycle before the rising edge of the clock. → 20 ns/div. and ↑ 500 mV/div.

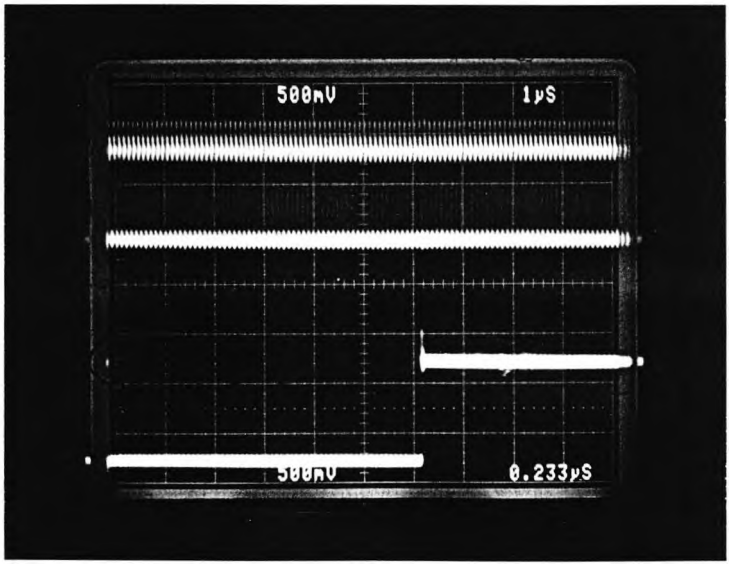


Fig. 7.17 The clock signal (upper trace) and the A6 signal (lower trace) as above, but on a wider time scale.

acquisition.

Fig. 7.18 shows the state of the address lines while the computer was reading the contents of the RAMs in the recorder unit. This figure shows the address line A6, amongst other address lines, which change state and the RAMCLK arrives one half of a clock cycle after the address lines have changed state. Fig. 7.19 shows the condition as Fig. 7.18 but on a wider time scale.

3. State analysis of data at input and output of the RAMs.

The object of this exercise was to locate the source of the "addressing error" within the recorder unit. Monitoring the data at the input of the RAMs using the state analyser revealed that the 'correct' data, i.e. without any "glitches", is set up at the input of the RAMs. This proves that the data is correct up to the output of the latches (U19 & U20) or the input of the RAMs. However, during the 'read' mode, the data acquired by the state analyser at the output of the RAMs was the same as that retrieved by the computer. Therefore the cause of the addressing error is likely to be within the RAMs of the recorder unit.

4. State analysis of input and output data and address input of the RAMs.

The aim of this analysis was to correlate the relocated data and the corresponding address. To do this the 'correct' data at the input of the RAMs and the data at its output were monitored as well as the corresponding address lines. The following was obtained from the state analyser and the data retrieved by the Personal Computer (PC).

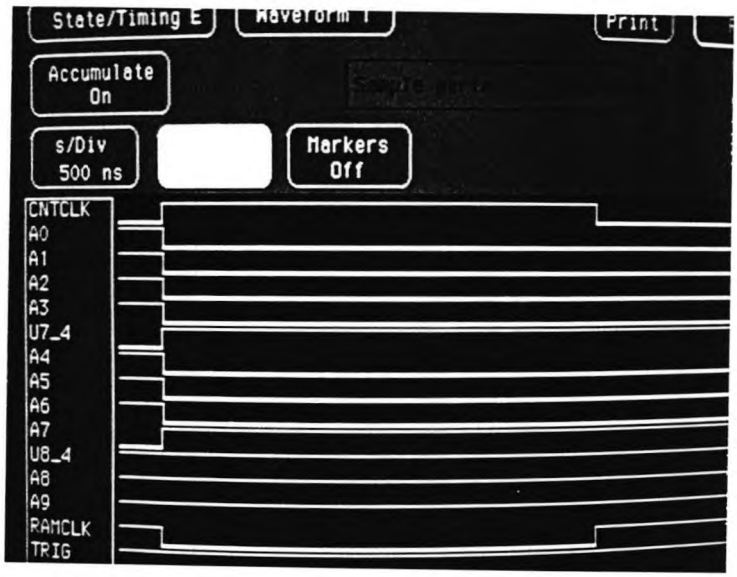


Fig. 7.18 The timing diagram of the RAM address inputs during the 'read' mode. The address lines A0-A9 changing from 11 0111 1111 to 11 1000 0000.

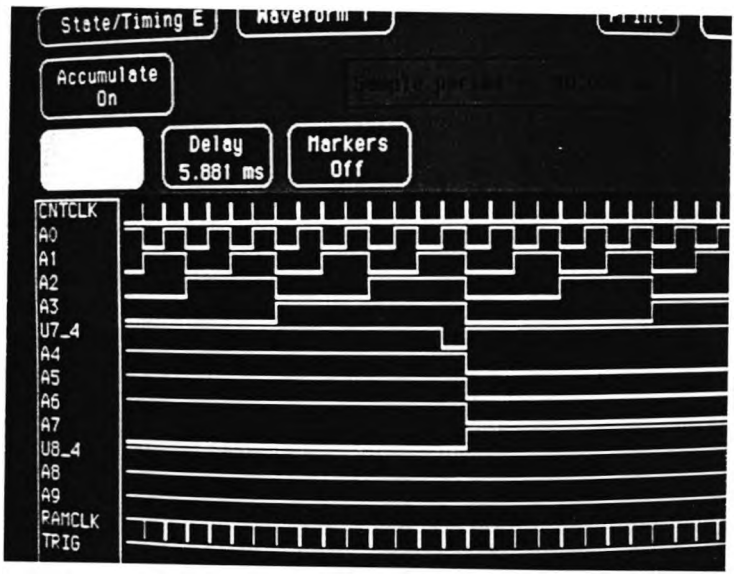


Fig. 7.19 The above timing diagram on wider time scale.

----------LOGIC ANALYSER----------				PC OUTPUT
Instrument Address (decimal)	DATA (RAM input) (decimal)	RAM (hex)	Address (binary) $A_9..A_6$ A_5 ..... A_0	DATA (decimal)
-497	132	27F	1001 111111	132
-496	134	280	1010 000000	228
-495	135	281	1010 000001	135
-433	227	2BF	1010 111111	227
-432	228	2C0	1011 000000	234
-431	229	2C1	1011 000001	229
-369	235	2FF	1011 111111	235
-368	234	300	1100 000000	146
-367	234	301	1100 000001	234
-305	148	33F	1100 111111	148
-304	146	340	1101 000000	45
-303	145	341	1101 000001	145
-241	046	37F	1101 111111	46
-240	045	380	1110 000000	17
-239	045	381	1110 000001	45
-177	016	3BF	1110 111111	16
-176	017	3C0	1111 000000	85
-175	017	3C1	1111 000001	17
-113	083	3FF	1111 111111	83
-112	085	000	0000 000000	192
-111	087	001	0000 000001	87

Table 7.2 Comparing the address and data monitored on the logic analyser and those retrieved by the PC from the recorder unit.

The above data and address information show that:

1. correct data is presented to the data inputs of the RAMs of the recorder unit,

2. the address count also increments correctly at the address input of the RAMs,

3. in the vicinity of the 'glitch' both the state of the input data and that of the address lines are correct and show no sign of faulty operation.

As far as the address inputs of the RAMs are concerned the following may be

observed:

1. a 'glitch' occurs every time A6 changes together with the subsequent change of state in A7, A8 and A9.

2. at the instance of the 'glitch', A0-A5 always remain the same.

Since the "glitches" are not the only ones to have the 2^6 address bit component, it is difficult to reconcile this with an address error caused by the address generating circuit. This conclusion is reinforced by the logic analyser tests described above. It was thought that these errors might be associated with the carry-bit transfer between the 4-bit counters of the address generating circuit, but experimental results show that they occur when there is no carry-bit transfer between the counters. It may be concluded that correct interpretation of the address data is not being made at the RAM. Inside the RAM chips, the address data is decoded in order to generate data for a series of rows and columns so that data is stored in a particular location. It could be that the address decoding circuit, driven by A6-A9, malfunctions and for every increment in the A6-A9 lines, the first address location is, in effect, 'lost'.

Unfortunately, circuit diagrams for the RAMs used in the recorder unit were not available from the manufacturer (Vitesse), nor were any more samples of these RAMs. The manufacturer had stopped producing these RAMs, but instead they are marketing slower version RAMs with different address/bit organisation. The data sheets made available by Vitesse are given in Appendix J.

7.6 Chopped-Impulse Test of the Recorder Unit

The second phase of testing the recorder system was using chopped impulse input signals. The repetitive chopped impulse tests were more difficult than the corresponding ADC-FOL-DAC tests.

The instability of the ADC driver made it extremely difficult to obtain records because we needed the DAC output display for the adjustment of the ADC driver and changing the circuit to the recorder unit arrangement took several minutes, during which time the ADC driver had drifted from the adjustment. In the event, a continuous series of records were obtained as the driver drifted into and out of the stable region. Some of these records are shown in Figs. 7.20, 7.21 and 7.22. In Fig. 7.20 a number of 'irregular' spikes can be seen that result from the 'partial disintegration' of the ADC output which is due to the ADC driver instability. Only five 64-spaced glitches can be noticed in this record. This is because most of the record is a straight line and therefore the misplaced data will not be noticeable since all the data for the straight line are the same. Figs. 7.21 and 7.22 show instances of more severe instability captured by the recorder unit. Better and more reliable results would be produced once the stability difficulty of the ADC driver has been resolved.

The records were taken with a sampling clock frequency of 100 MHz and so the 1024 samples represent a period of 10.24 μs. The digital codes of 0 and 255 correspond to -250 mV and 0 mV respectively at the input of the ADC driver. This relationship of the digital codes and the signal amplitude is the characteristic of the ADC output.

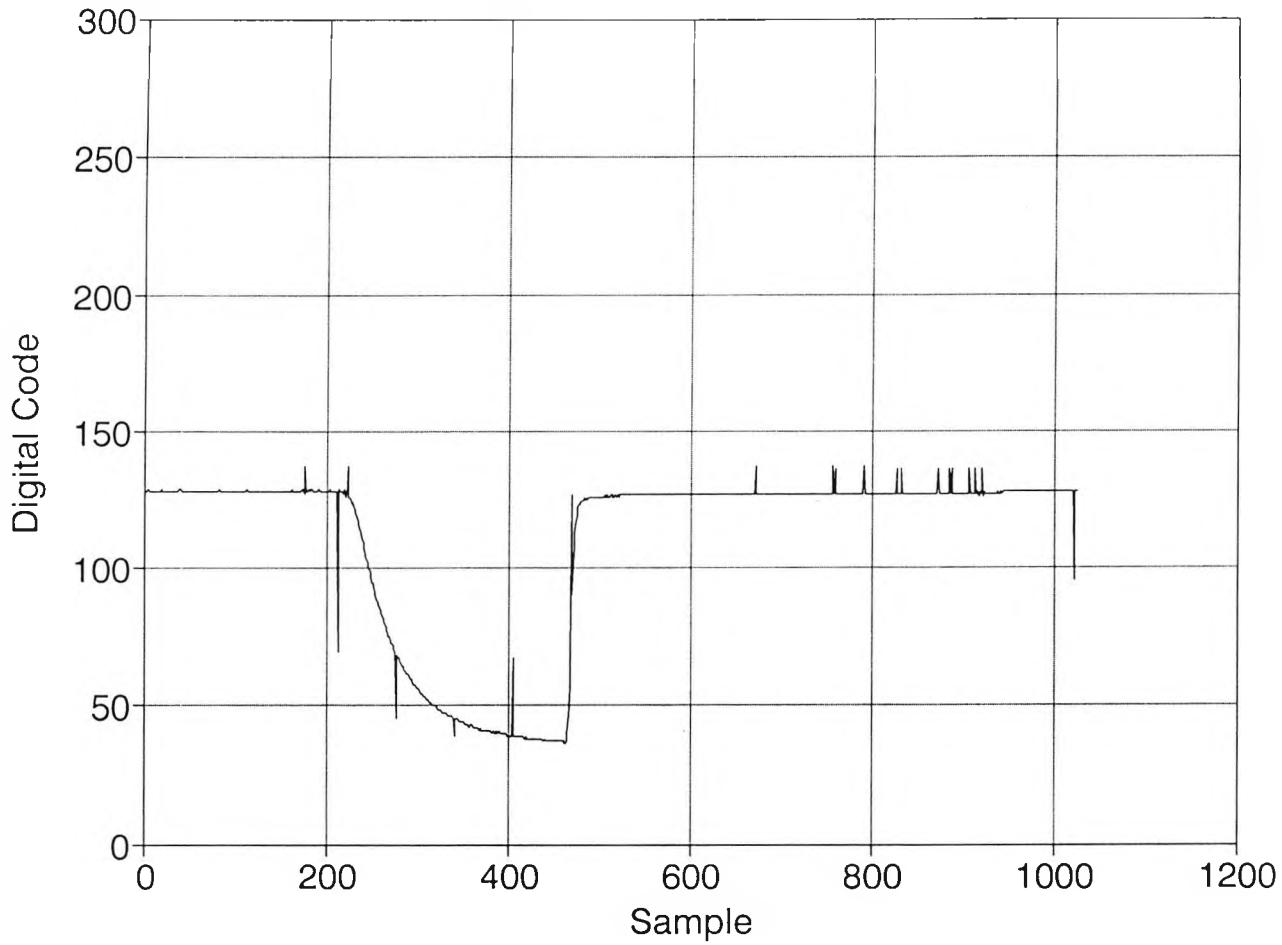


Fig. 7.20 A record of a 'partially disintegrated' chopped impulse captured by the recorder unit.

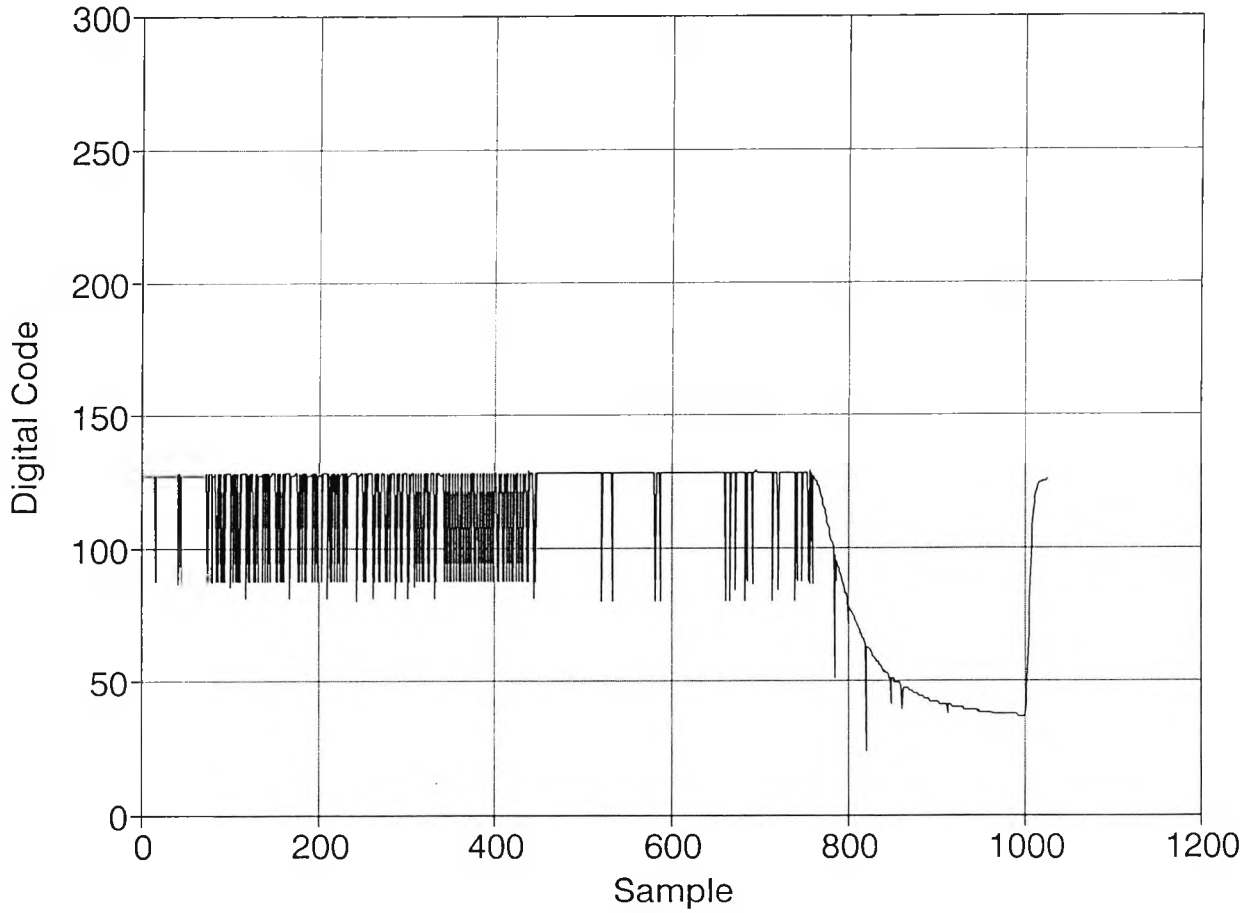


Fig. 7.21 Example of a 'disintegrated' output captured by the recorder unit.

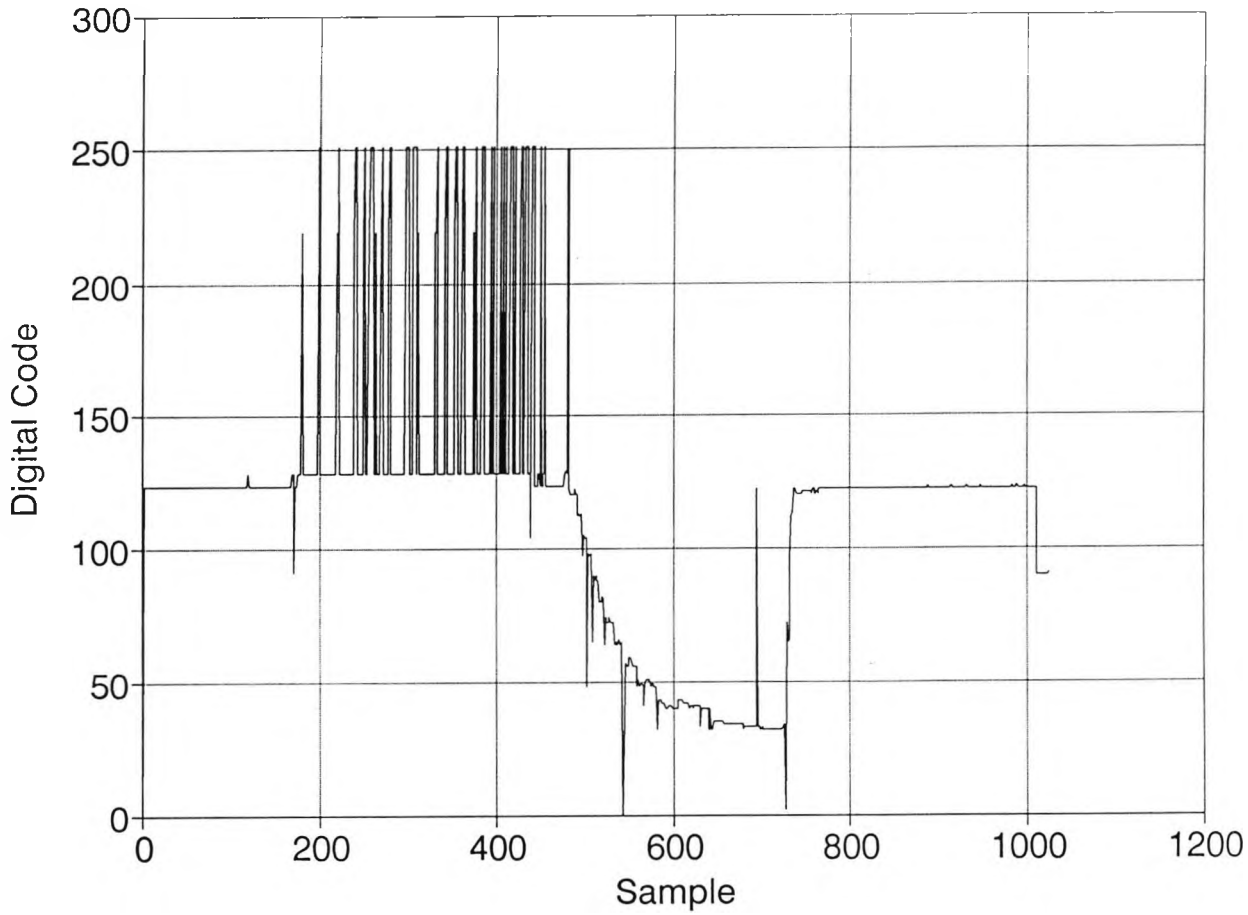


Fig. 7.22 Another example of the 'disintegrated' signal.

7.7 Summary

The results of the tests carried out on the units and the complete system of the DOCTR may be summarised as follows:

The ADC-FOL-DAC system was tested successfully for sinusoidal input signals and frequency spectrum analysis of the DAC output revealed low levels of harmonics which are due to the non-linearity effects of the converters (the ADC and the DAC).

The ADC-FOL-DAC system was also tested, successfully, for chopped-impulse inputs with chop time of 100 ns. The driver of the ADC chip was unstable and this resulted in the distortion of the DAC output unless it was adjusted.

The performance of the capture unit screening was tested in the electrically harsh environments produced by the operation of HV impulse generator at 800 kV.

The complete DOCTR system was first tested for sinusoidal inputs. This revealed a number of "glitches", spaced at 64 address locations apart. This phenomenon appeared every time there was an increment in the address values of A_6-A_9 only. The input and output data and the address inputs to the RAMs were monitored for possible sources of error. Correct data arrived at the input of the RAMs and there were no errors in addressing the address inputs of the RAMs. Only the output of the RAMs revealed these so called "glitches" and it was therefore concluded that this phenomenon originated within the RAMs.

The data retrieved by the computer was the same as that monitored at the output of the RAMs. This showed that the computer interrogation process operated correctly and that the software specifically written for this purpose ran successfully.

Finally the high frequency performance of the Recorder unit vindicates its circuit design and that results such as Fig. 7.14 and Fig. 7.15 confirm the simulation results carried out on the recorder circuit design (Fig. 5.14).

CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 Conclusions

A review of the measurement systems for use in electrically harsh environments in chapter 2 revealed the shortcomings of those systems for the recording of transient signals in such surroundings. Depending on their design they were grouped into two main categories:

One type of measurement system was the conventional conductor-connected system which presented significant operational problems in noisy environments.

The other type of measurement system used optical fibre links which avoided some of the problems. The optically coupled systems were grouped into two categories

depending on whether analogue or digital links were used.

Analogue links suffer from non-linearity of the optical transmitter as well as the optical fibre cable. The non-linearity characteristics of the optical transmitter varies with temperature and ageing whereas those of the optical fibre are affected by strains too. These effects are immediately reflected on the analogue transmission of the signal and therefore result in the distortion of the latter. In systems using analogue FOLs, therefore, the link itself could be the source of measurement errors and this has been encountered in practice.

The measurement systems using digital FOL reviewed had various characteristics, but were not suitable for fast impulse measurements. In one system, although it had very wide bandwidth, but because of the analogue-to-digital conversion technique used, the input signal to the system needed to be repetitive. The other system which used a digital FOL for surge recording had a sampling rate of only 5 MS/sec.

At the outset in our initial analysis of the requirements of the measurement problem we were aware that some attempts at traceable measurements of smaller signals produced within a hostile environment had to be made in a simple and inexpensive manner. Later experience has indicated that many simultaneous measurements may be required during a prolonged test period of many hours. The processing of these signals, either to correct for the system response or merely to process the experimental test data, itself demands a linear system in addition to that needed as a basis for traceable measurement. The system designed meets these requirements in that the digital transmission and recording system is adequately linear for its purpose. With such a digital system, the only link in the chain of traceability is the ADC and it is the traceable calibration of this which dominates the uncertainty of the overall measurement.

The DOCTR system suggested in this work combines four important features for the measurement of random fast transients in electrically hostile environments.

- The transient signal is digitised at 'source' in order to eliminate any possible source of error due to analogue transmission.

- With the system divided into two parts, an optical link is used to allow communication between the two parts. The optical link not only provides immunity from EM interference for the data being transmitted, but electrical isolation is also established between the two parts. A digital link is used since, except in extreme cases, it is almost insensitive to the non-linear characteristics of the transmitter and the optical fibre (to which analogue link is very susceptible).

- A significant feature of the system is its speed of operation which enables the capture of fast transients with the digitisation rate of 100 MS/sec, the transmission rate through the optical link and the recording rate in the RAM unit are also at 100 MS/sec.

- Another important aspect of this system is the ability to perform 'single-shot' measurement or random transient capture. At such speeds, the state of the incoming data is continually monitored and when a preset condition is encountered, the required signal is recorded. In this way no external pre-event trigger is required. The control circuit of the recorder unit may be programmed in order to record any length of the 'pre-event' history of the transient. By similar means, the 'trigger threshold level' may be programmed to allow the recording of the signal, say , in the presence of background noise. With the optical link and the recorder units being linear digital systems, only the ADC unit of the system needs to be calibrated and therefore traceable measurements are easier to perform using such a system.

In developing the DOCTR system, a review was carried out of the various types of digitisers commercially available and those suitable for such applications as this. The performance characteristics of the ADC used for this application were also discussed. In developing the fibre optic link needed in this system, a survey was made of the

optical fibre cables and their characteristics discussed. The various types of optical sources and detectors used in fibre optic communication were also considered their characteristic discussed and subsequently the most suitable for this application selected. A review was also presented of the circuit designs for the driver and receiver circuits for the optical link. The different design philosophies of the circuits and their particular advantages were outlined. The FOL unit was shown to perform well under harsh electrical conditions. We have also shown that the screening system of the capture unit is adequate. The degree to which the signal converter produces valid signals and/or pick-up is, to a large degree, part of the problem of providing the measurement signal.

The eventual simulation results of the recorder unit at the clock speed of 100 MHz confirmed the validity of the circuit designs taking into account the different probabilities of the combinations of the various propagation delays through each component in the circuit. During the process of simulations of the transmitter and receiver circuits using SPICE program and also when simulating the recorder unit circuit using System-HILO 2 software, in both cases simulation errors were detected in the corresponding results which were tracked down to the particular faults in the each program.

The sinusoidal and chopped-impulse tests carried out on the ADC-FOL and the DOCTR systems revealed the potential of the DOCTR system in capturing rapidly changing signals accurately. Although these tests pointed out the instability of the DAC driver and also the "glitch" problem in the RAM chips, the data acquisition capability of the Recorder unit confirmed the validity of its circuit simulation results obtained earlier.

8.2 Suggestions For Further Work

There are numerous avenues for extending the work reported in this thesis to further develop the DOCTR system.

During the course of the development of the DOCTR system, a number of improvements were realised that could be implemented for the next generation of the system.

Although this instrument was designed for data rates of up to 100 MS/sec, there are suggestions that higher data rates are preferred. As there are currently ADCs which are capable of digitisation rates of 300 MS/sec with 8-bit resolution and the present fibre-optic link is capable of 320 MS/sec, this only leaves the need for RAM devices capable of working at this data rate. In the absence of high speed RAMs, 300 MS/sec data recording could be achieved by using the available lower speed RAMs in an interleaved circuit arrangement.

With the continuing advancement in material and fabrication technologies, many aspects of the hardware may be improved upon which would give greater flexibility to the measurement procedure. However, one aspect that could be immediately implemented without the introduction of the latest technology, is to implement a multi-probe system where several capture units communicate with one PC. By this means simultaneous measurements can be made at different locations and all the measurement data can be retrieved by the PC for further analysis. In applications such as aircraft lightning testing the data from the various points of interest can be compared and processed immediately and economically. With present recording systems using analogue FOLs, such multi-point measurement are done with as many CRO's or recorders as the number of capture units. In such cases, in addition to the greater cost of the hardware systems, comparison of the data from the various measurement points is a tedious process.

With the introduction of higher capacity RAMs to be made shortly [Sony, 1993], such RAMs could be used in the next generation of the DOCTR system to make greater record lengths possible. With the recent developments in CMOS fabrication technology, high speed CMOS RAMs [IDT, 1992] are becoming available which have the advantage of low power consumption. With such RAMs, the idea of having the

recording unit housed in the capture unit should be explored. In this case a low speed single channel FOL may be used to link the capture unit and the PC. At the moment the size of the recorder unit circuit board is about 8"×9", which is too large to accommodate in a relatively small capture unit. However, with the progress made in the VLSI fabrication process and the widespread availability of the ASIC facilities (Application Specific Integrated Circuits), a digitiser unit might be implemented on a hybrid integrated circuit with a high speed CMOS RAM unit on board. This will also have the advantage of miniaturising the capture unit. The possibility of integrating the recorder unit into the capture unit to produce a low power consumption miniature capture unit must be pursued.

Appendix A PECL-to-ECL Matching

The arrangement for matching the PECL output to standard ECL input is shown in figure A.1.

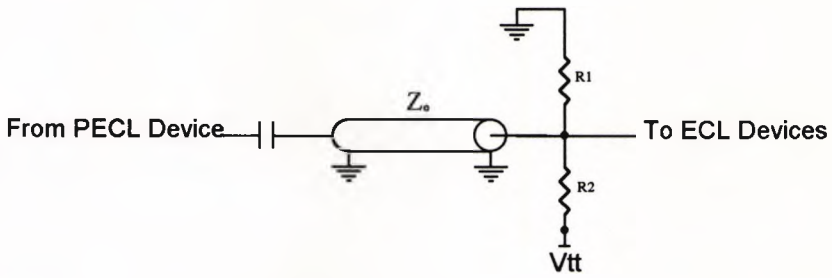


Figure A.1 Arrangement for matching PECL to ECL logic

The requirement at the receiving of the transmission line is that the line is matched and the correct bias is established for the ECL device. Therefore we must have

$$R_1 \| R_2 = Z_o \tag{1}$$

$$\left(\frac{R_1}{R_1 + R_2} \right) \cdot V_{tt} = V_{ref} \tag{2}$$

where Z_o = 58 Ω , V_{ref} =-2 V and V_{ref} = -1.3 V (for ECL device [Motorola, 1986])

Solving equations (1) and (2) gives R_1 =160 Ω and R_2 =91 Ω .

Appendix B ECL-to-GaAs Matching

The circuit of figure B.1 used to match ECL devices to GaAs-based devices.

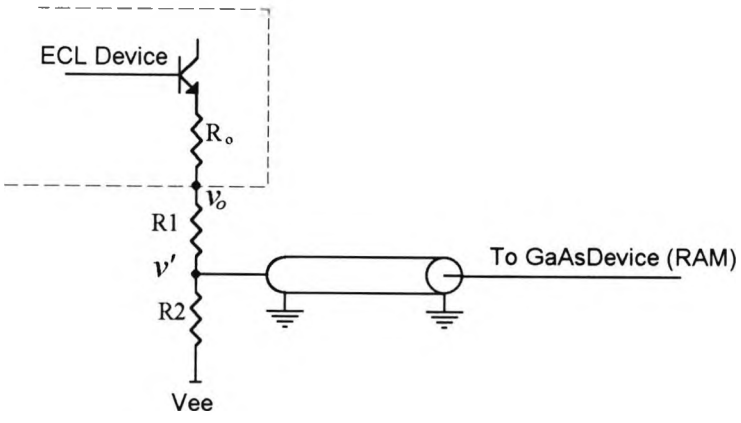


Fig B.1 Arrangement For Matching Standard ECL to GaAs-based Devices

Three criterion need to be satisfied:

1. DC Condition

$$\frac{(v' - V_{ee})}{R_2} = \frac{(v_o - V_{ee})}{R_1 + R_2}$$

$$\therefore v' = \frac{R_2}{R_1 + R_2}(v_o - V_{ee}) + V_{ee} \qquad (1)$$

2. Line Matching

$$(R_o + R_1) \| R_2 = Z_o \qquad (2)$$

3. Transient Condition

$$\frac{\delta v_e}{R_o + R_1 + (R_2 \| Z_o)} (R_2 \| Z_o) \times 2 = \delta v_{GaAs} \quad (3)$$

where $\delta v_{GaAs} = 0.92 \delta v_o$

For ECL logic High, v_O=V_{oHmin}=-0.98 V [Motorola, 1986]

From equation (1)

$$v' = 4.22\left(\frac{R_2}{R_1 + R_2}\right) - 5.2 \quad (1A)$$

For ECL logic Low, v_o=V_{oLmax}=-1.63 V [Motorola, 1986]

From equation (1)

$$v' = 3.57\left(\frac{R_2}{R_1 + R_2}\right) - 5.2 \quad (1B)$$

The noise margin (NM) for the High and Low logic levels are given by

$$NM_{high} = V_{oHmin} - V_{iHmin} \quad (4)$$

$$NM_{low} = V_{iLmax} - V_{oLmax} \quad (5)$$

where V_{iHmin} =-1.4 V and V_{iLmax} = -1.8 V for GaAs-based device.

To have equal noise margins for the low and high logic levels at the GaAs input we must have

$$NM_{high} = NM_{low} \quad (6)$$

Substituting for equation (6), using (1A) and (1B),we have

$$(1A) + 1.4 = -1.8 - (1B) \quad (7)$$

Solving equation (7), we have

$R_2 = 12.2\ R_1$ (8)

Substituting equation (8) in equation (2), we have

$R_1 = 56\ \Omega$ and $R_2 = 687\ \Omega$

Equation (3) may be rewritten as

$$\frac{R_2 \| Z_o}{R_o + R_1 + (R_2 \| Z_o)} = 0.46 \quad \text{(2A)}$$

Equation (2A) may be used to check the derived values of R_1 and R_2, given that

$R_O = 7\ \Omega$ and $Z_O = 58\ \Omega$.

Appendix C GHDL and WDL Programmes used for HILO Simulation

```
CCT ECL HEX CONTRLS (INPUT DA[11:0],DB[8:0],PR[11:0],CLK100,CE,REARM,
                     REARMBAR,CPUCLK,EN,AS2,DFF,R,CIA,CIT,I[11:0],CC,
                     OUTPUT A[11:0],D[11:0],TA[11:0],RAMCLK,COA,COT);

  MC10103P
  U12 (
       VCC1,
       ,
       ,
       ,
       ,
       ,
       ,
       VEE,
       TA10BAR,
       N00028,
       TA[10],
       TA[10],
       TA[10],
       N00027,
       ,
       VCC2
       );

 MC10103P
 U13 (
      VCC1,
      TIMECLK,
      LTCHCLK,
      N00009,
      CLK,
      CLK,
      N00009,
      VEE,
      RAMCLK,
      ,
      ,
      CLK,
      N00009,
      ,
      ADRSCLK,
      VCC2
      );

MC10104
U10 (
     VCC1,
     AS1,
     TS1,
     TA[10],
     CE,
     N00027,
     REARMBAR,
     VEE,
     ,
     CLK100,
     TA10BAR,
     CPUCLK,
     TA[10],
     CLK,
     N00009,
     VCC2
     );
```

```
MC10131
U14 (
     VCC1,
     ,
     ,
     ,
     ,
     ,
     ,
     VEE,
     CC,
     OFF,
     TRIG,
     REARM,
     R,
     ,
     N00028,
     VCC2
     );

MC10176P
U19 (
     VCC1,
     D[6],
     D[7],
     D[8],
     DA[6],
     DA[7],
     DA[8],
     VEE,
     LTCHCLK,
     DA[9],
     DA[0],
     DA[5],
     D[9],
     D[0],
     D[5],
     VCC2
     );

MC10176P
U20 (
     VCC1,
     D[4],
     D[1],
     D[10],
     DA[4],
     DA[1],
     DA[10],
     VEE,
     LTCHCLK,
     DA[11],
     DA[2],
     DA[3],
     D[11],
     D[2],
     D[3],
     VCC2
     );

MC10H136
U4 (
     VCC1,
     TA[2],
```

```
      TA[3],
      N00022,
      PR[3],
      PR[2],
      REARMBAR,
      VEE,
      TS1,
      CIT,
      PR[1],
      PR[0],
      TIMECLK,
      TA[0],
      TA[1],
      VCC2
      );

MC10H136
U5 (
      VCC1,
      TA[6],
      TA[7],
      N00025,
      PR[7],
      PR[6],
      REARMBAR,
      VEE,
      TS1,
      N00022,
      PR[5],
      PR[4],
      TIMECLK,
      TA[4],
      TA[5],
      VCC2
      );

MC10H136
U6 (
      VCC1,
      TA[10],
      TA[11],
      COT,
      PR[11],
      PR[10],
      REARMBAR,
      VEE,
      TS1,
      N00025,
      PR[9],
      PR[8],
      TIMECLK,
      TA[8],
      TA[9],
      VCC2
      );

MC10H136
U7 (
      VCC1,
      A[2],
      A[3],
      N00002,
      I[3],
      I[2],
```

```
      AS2,
      VEE,
      AS1,
      CIA,
      I[1],
      I[0],
      ADRSCLK,
      A[0],
      A[1],
      VCC2
      );

MC10H136
U8 (
      VCC1,
      A[6],
      A[7],
      N00008,
      I[7],
      I[6],
      AS2,
      VEE,
      AS1,
      N00002,
      I[5],
      I[4],
      ADRSCLK,
      A[4],
      A[5],
      VCC2
      );

MC10H136
U9 (
      VCC1,
      A[10],
      A[11],
      COA,
      I[11],
      I[10],
      AS2,
      VEE,
      AS1,
      N00008,
      I[9],
      I[8],
      ADRSCLK,
      A[8],
      A[9],
      VCC2
      );

MC10H166P
U21 (
      VCC1,
      TRIG,
      ,
      N00034,
      N00035,
      DA[5],
      DB[5],
      VEE,
      DA[8],
      DB[8],
```

```
     DB[7],
     DA[7],
     DA[6],
     DB[6],
     EN,
     VCC2
     );

MC10H166P
U22 (
     VCC1,
     N00035,
     N00034,
     DB[0],
     DA[0],
     DA[1],
     DB[1],
     VEE,
     DA[4],
     DB[4],
     DB[3],
     DA[3],
     DA[2],
     DB[2],
     EN,
     VCC2
     );


WIRE     N00002,N00008,N00009,N00022,N00025,N00027,N00028,N00034,N00035;

INPUT    DA[11:0],DB[8:0],PR[11:0],CLK100,CE,REARM,REARMBAR,CPUCLK,EN,AS2,I[11:0];
INPUT0   DFF,R,CIA,CIT,CC;
OUTPUT   A[11:0],D[11:0],TA[11:0],RAMCLK,COA,COT;

SUPPLY0  VEE;
SUPPLY1  VCC1,VCC2;

ENDCIRCUIT
```

```
WAVEFORM CONTRL5;
INPUT  DA[11:0] DB[8:0] PR[11:0] CLK100 CPUCLK EN CE AS2 CIA CIT REARM REARMBAR I[11:0] DFF R CC;
OUTPUT  A[11:0] D[11:0] TA[11:0] RAMCLK COA COT;
WIRESET  CONTROL_LINES IS INPUT (EN,CE,AS2,REARM,REARMBAR,CPUCLK);

INTERVAL 5;
DELAYSCALING NANO;
BASE HEX;

PROCESS SIGNAL (INPUT DA[11:0]);
INTERVAL 10;
        BEGIN
        DA[11:0]:=0;
                    EXACTLY 19 TIMES DO
                                        INC (DA[11:0]);
                                    ENDDO
        END
ENDPROCESS SIGNAL;

PROCESS CLOCK (INPUT CLK100);
INTERVAL 5;
        BEGIN
        CLK100:=0;
                EXACTLY 19 TIMES DO          ***we need 910 times
                                    CLK100:= 0;
                                    CLK100:= 1;
                                ENDDO
        END
ENDPROCESS CLOCK;


   BEGIN
        POWERON;
        CIA:=0 CIT:=0 R:=0 DFF:=0 CC:=0;


        CLOCK (CLK100) SIGNAL (DA[11:0]);

        DB[8:0]:= HEX E  PR[11:0]:= HEX 33;

;
        CONTROL_LINES:= HEX 24;   ***COUNTERS IN PRESET MODE
;
        CONTROL_LINES:= HEX 25;   ***INPUT DATA LOADED INTO COUNTERS USING CPUCLK
;
        CONTROL_LINES:= HEX 24;   ***IN PRESET MODE
;
        CONTROL_LINES:= HEX 0A;   ***SYSTEM REARMED, COUNTER SET TO UP COUNT AND COMPARATOR ENABLED




   END
ENDWAVEFORM
```

Appendix D ADC Circuit Board Diagrams

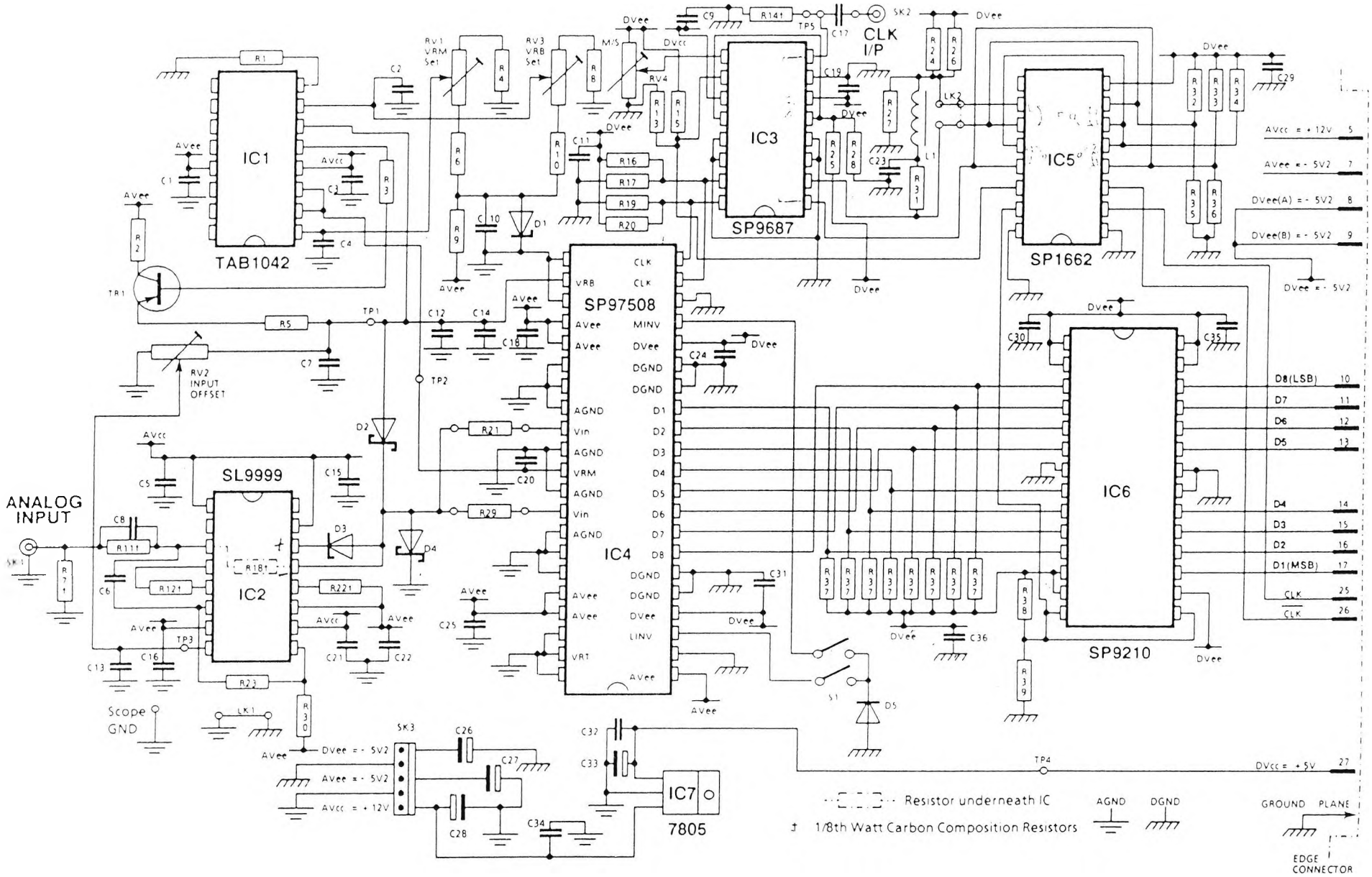


Fig D.1 SP97508 ADC Evaluation Board Circuit Diagram

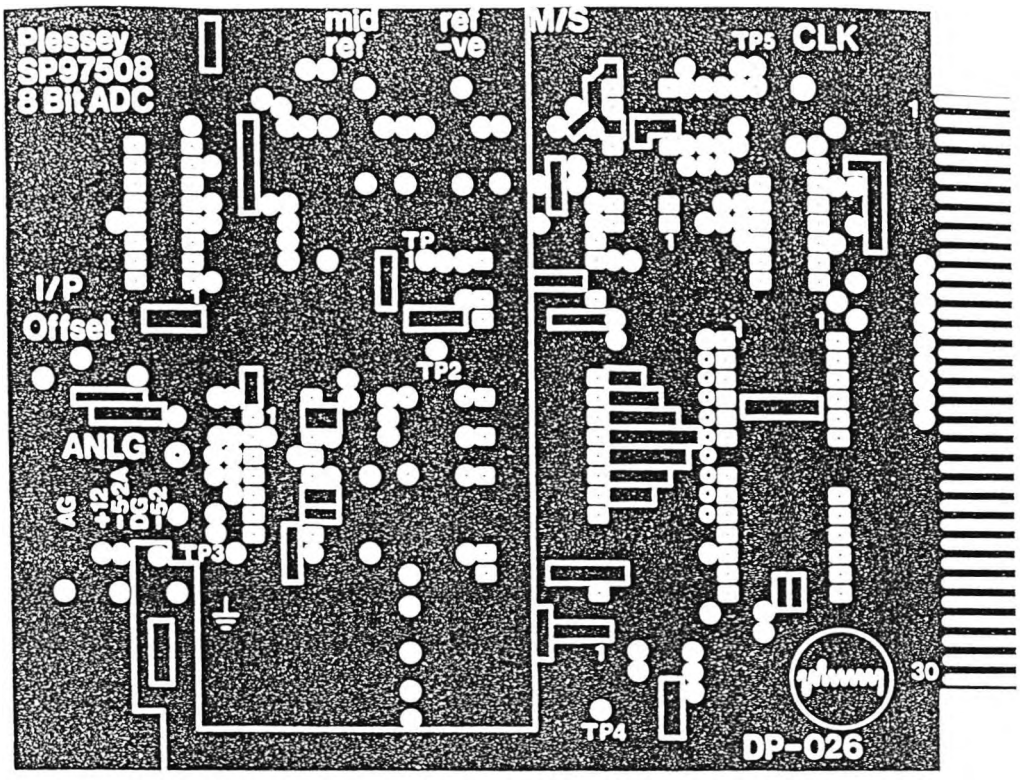


Fig D 2(a) ADC Board (ground plane)

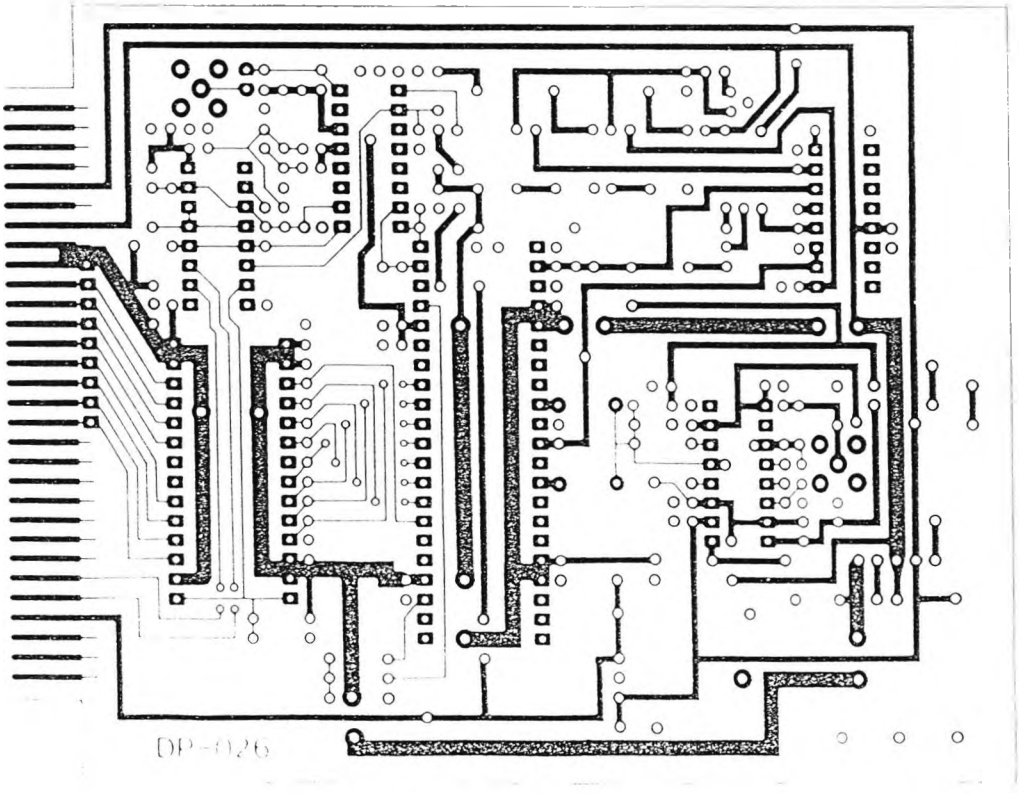


Fig D 2(b) ADC Board (track side)

Appendix E Skin Depth Calculation

The skin depth is defined as the penetration in to the conductor at which the magnitude of the current has decreased to $1/e$ (36.8%) of its value at the surface; since $i_z = i_0 e^{-x/\delta} e^{-jx/\delta}$

For a plane conductor, it can shown that the skin depth is given by [Ramo, et al, 1965.]:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

For copper; $\sigma = 5.8 \times 10^7$ and $\mu = 4\pi \times 10^{-7}$

$$\therefore \delta = \frac{66}{\sqrt{f}} \; mm$$

Therefore for copper plane, the skin depth at

f = 100 MHz is 6.6 μm

and at f = 1 GHz is 2.0 μm.

The skin depth equal to the copper sheet thickness of 0.6 mm corresponds to a frequency of 12 kHz.

Appendix F Cutoff Waveguide Design

A wave propagating along a uniform guiding system may be described in terms of the propagation factor $e^{(jwt-\gamma z)}$ where the propagation constant γ indicates the properties of the wave, degree of attenuation etc. It can be shown that for any dielectric region which is completely closed by perfect conductors the constant γ is given by [Ramo et al, 1965.]:

$$\gamma = \frac{2\pi}{\lambda_c}\sqrt{1-\left(\frac{f}{f_c}\right)^2} \qquad (1)$$

where f = operating frequency

f_c = cut off frequency

λ_c = cut off wavelength

Using the general solution of Maxwell's equations for dielectric region, it is possible to derive the expression for the electric and magnetic field components of waves. Solving for the boundary conditions for a perfectly conducting guide of a circular cross section we obtain the expression for the cut off wavelength [Ramo et al, 1965].

$$\lambda_c = \frac{2\pi r}{P_{nl}} \qquad (2)$$

where P_{nl} is the root of the Bessel function satisfying the boundary condition of a circular waveguide of radius r. The value of P_{nl} depends on the type of the wave (magnetic or electric) and the mode of transmission of the wave.

For a 1 cm diameter circular waveguide, equation (2) is rewritten :

$$\lambda_c = \frac{\pi}{P_{nl}} \text{ cm} \qquad (3)$$

but $$f_c = \frac{v}{\lambda_c}$$

$$= \left(3\times 10^{10} \text{ cm/s}\right)/\left(\pi/P_{nl}\right)$$

$$= \left(3 \times 10^{10}\right) P_{nl} / \pi \ \text{s}^{-1}$$

$$\therefore \quad f_c = 9.55\, P_{nl} \ \text{GHz} \tag{4}$$

The frequencies involved in an EM environment such as the HV laboratory are much smaller than the cut off frequencies of different modes of waves in a 1 cm diameter guide. Therefore the attenuation expression of equation (1) reduces to

$$\gamma = \frac{2\pi}{\lambda_c} \ \text{nepers/meter} \tag{5}$$

Substituting for λ_c from (2) in (5) we have

$$\gamma = \frac{P_{nl}}{r} \ \text{nepers/meter} \tag{6}$$

But

$$\gamma_{np} = \ln 10 \times \gamma_{bel}$$

$$\gamma_{bel} = \frac{\gamma_{np}}{\ln 10}$$

or $$\gamma_{dB} = 20 \times \frac{\gamma_{np}}{\ln 10}$$

$$= 8.7 \gamma_{np}$$

$$\therefore \gamma_{dB} = 8.7\left(P_{nl} / r\right) \quad \text{dB/m} \tag{7}$$

For an 8 cm length circular waveguide of 1 cm diameter the above expression of attenuation is rewritten as

$$\gamma_{\text{dB}} = 139\, P_{nl} \ \text{dB} \tag{8}$$

For a TE_{11} wave, say, the attenuation achieved through this waveguide at frequencies well below its cut off frequency is

$$\gamma_{\text{dB}} = 139 \text{ x } 1.84 = 256 \text{ dB}.$$

This waveguide therefore provides adequate protection for the probe unit by attenuating the interfering signal to an insignificant level inside the box. The level of

attenuation achieved by this method is better than that of a screened room which is about 100 dB.

The cut-off frequencies and attenuations of this circular waveguide for different modes of TE and TM waves are given in the table below:

Wave	TM_{01}	TM_{02}	TM_{11}	TE_{01}	TE_{11}
P_{nl}	2.405	5.52	3.83	3.83	1.84
f_c (GHz)	23	52.7	36.6	36.6	17.6
γ (dB) (for 8 cm)	334	767	532	532	256

Appendix G Interface Software

```
10    REM       ***filename is RW3
20    DIM       D(1024)
30    OUT       &H303, &H80
40    OUT       &H307, &H9B
50    OUT       &H302, &H30
60    INPUT     'ENTER REQUIRED NO. OF PRETRIGGER SAMPLES:',P
70    OUT       &H300, P
80    OUT       &H302, &H31
85    OUT       &H302, &H30
90    INPUT     'ENTER REQUIRED THRESHOLD LEVEL:',T
100   OUT       &H301, T
110   OUT       &H302,&H32
115   OUT       &H302,&H30
120   INPUT     'ENTER FILENAME:',F$
130   INPUT     'ARE YOU READY TO START RECORDING? (Y/N)',R$
140   IF        R$='N' GOTO 30
150   OUT       &H302, &H10
160   OUT       &H302, &H18
170   OUT       &H302, &H1C
180   OUT       &H302, &H18
190   OUT       &H302, &H10
200   PRINT     'THE SYSTEM HAS BEEN RE-ARMED.'
210   A10=INP(&H305)
220   IF        A10=&H0 GOTO 210
230   OUT       &H302, &H20
240   PRINT     TIME$
250   OPEN      'O',£1,F$
260   FOR       L=1 TO 1024
270   OUT       &H320, &H24
280   OUT       &H302,&H20
290   D(L)=INP (&H304)
300   PRINT     £1,D(L);
310   NEXT
320   CLOSE     £1
330   PRINT     TIME$
340   PRINT     'DATA HAS BEEN RETRIEVED FROM RAM AND
                STORED ON DISK'
350   INPUT     'DO YOU WISH TO ACQUIRE ANOTHER RECORD?
                (Y/N)',Q$
360   IF        Q$='N' GOTO 410
370   PRINT     'DO YOU REQUIRED NEW SETTING FOR THE NEXT
                RECORD? (Y/N)'
380   INPUT     IF (NO), THE PREVIOUS SETTINGS WILL BE USED:', W$
390   IF        W$='N' GOTO 120
400   IF        W$'Y' GOTO 30
```

```
410   INPUT     'DO YOU WISH TO READ A FILE?(Y/N)' J$
420   IF        J$='N' THEN END
430   INPUT     'ENTER NAME OF FILE TO BE READ:' M$
440   OPEN      'I', £1, M$
450   FOR       L=1 TO 1024
460   INPUT     £1, D(L)
470   PRINT     D(L);
480   NEXT
490   CLOSE     £1
500   GOTO      350
```

Appendix H Battery Supply Regulation and Monitoring

H.1 Optical Transmitter Supply Regulation

The nominal supply voltage required for the transmitters is -5.0V although the minimum acceptable voltage is -4.5V [BTD, 1990]. With the difference between the battery and regulated voltage being about 1V, it is important to use a low dropout voltage regulator for this application to allow proper operation under these conditions. The Low Dropout Regulator (LT1185) is used and this has an input to output voltage drop of [Linear Technology 1990]:

$$(0.25V + 0.25I_{out}) \qquad (1)$$

The circuit diagram for the voltage regulator is given in figure H.1.

The regulator features programmable output voltage and current. The output voltage is determined by the values of the regulating resistors R_1 and R_2 as given by

$$V_o = 2.37(R_1+R_2)/R_1 \qquad (2)$$

[for $R_1 = R_2 = 2.4k$, $V_o = -4.74V$]

The maximum output current is set by selecting the value of the current programming resistor R_3.

$$R_3 = 15/I_{max} \qquad (3)$$

[for $I_{max} = 1.5A$, then $R_3 = 10k$.]

For voltage monitoring, the low-voltage detector ICL7665S is used together with an LED to indicate low battery voltage. The circuit diagram for this is given in figure H.2. The detector monitors the changes in the battery voltage level output and can be set to indicate the low battery level as required.

R_4 and R_5 determine the threshold level at which the low- voltage detector flags an output. The threshold level is dictated by the minimum acceptable supply voltage to the device being powered. The relation between resistors and the threshold level is given by

$$V = 1.3\ (R_5 + R_4)/R_5 \qquad (4)$$

Since the battery output is being monitored, when setting the detector threshold level, the input-to-output voltage drop of the regulator must be taken into account. For I_{out}=1.5 A, using equation (1), the voltage drop is 0.625V. With the regulated voltage given above, the threshold level is -5.4 V. This gives R_4=15k and R_5=4.7k.

H.2 ADC Supply Regulator

For the -5.2V supply, a similar circuit is used for the regulator. In this case the supply voltage tolerance is +/-0.2V which is smaller than that of the optical transmitter. The corresponding values for the regulating resistors R_1 and R_2 are therefore

R_1 = 2.4k and R_2 = 2.7k

resulting in the regulated output of -5.04V.

The current limit for this supply is set to 1A by setting

R_3 = 15k.

The diagram for this circuit is similar to that of Fig H.1 but with different resistor values.

For low voltage monitoring, the same circuit is used as that of the optical transmitter supply, except that different threshold level is set for the detector to indicate. In this case the low voltage monitor is set to indicate is -5 -(1+1)/4 = -5.5 V. The nearest nominal values for the threshold resistors R_5 and R_4 are 33k and 10k respectively.

No voltage regulation is required for the +12V supply since the nominal output of the battery is the same as that required by the supply voltage. Only low voltage detection is needed and the threshold voltage is set at +11V which is acceptable for circuit operation. The circuit for the low-voltage detector for the 12V supply is similar to that of figure H.2. In this case the threshold resistors are 10k and 75k.

To conserve battery power a relay is remotely controlled through an optical fibre. A photodiode is used to convert the optical signal back to an electrical one and a high-current-gain Darlington pair drives the relay. The circuit diagram for the optical remote controlled relay is shown in figure H.3.

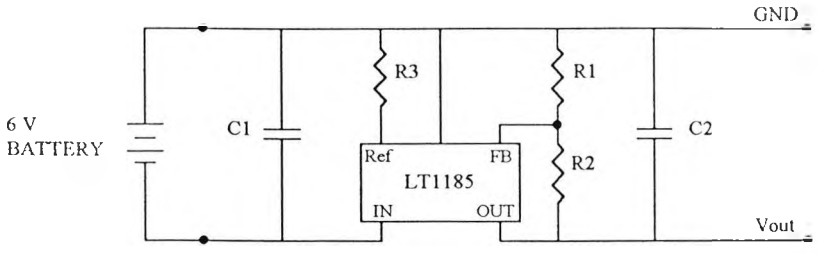


Fig H.1 Voltage regulator circuit diagram

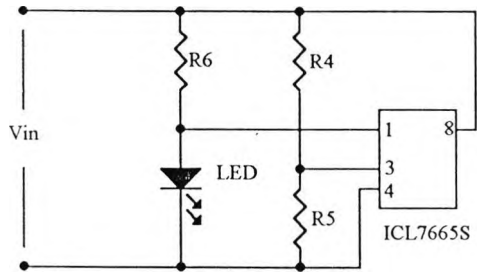


Fig H.2 Low voltage detector

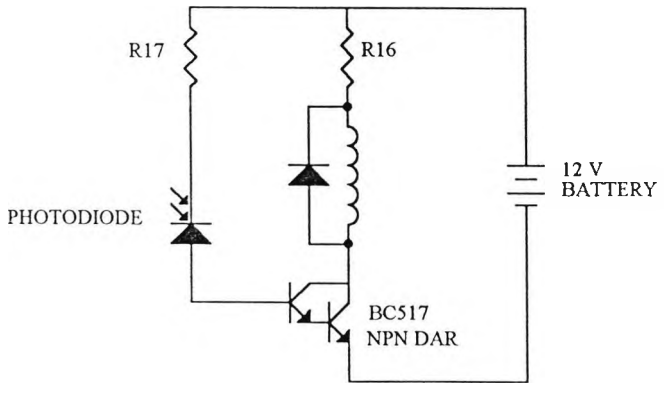


Fig H.3 Optically remote controlled relay circuit diagram

Appendix I Chopped-Impulse Circuit

The impulse was of double exponential form having a rise time of 1.2 μs and a time to fall to one half of the peak value of 50 μs. The circuit produced negative impulses.

With this circuit, the impulse wave could be chopped at any point from near its peak value to the tail of the wave. Another feature of this circuit is that the chop time could be determined, down to less than 100 ns, by adjusting the drive state of the chopping transistor.

The circuit is used in conjunction with a Philips square wave generator (PM 5775) which facilitates variable pulse width and delay. The repetition rate of the pulses of this circuit may be controlled by the Philips generator. The diagram for this circuit is shown in Fig. I.1.

In this circuit the capacitor C_1 is charged through R_3 and R_4 and when the transistor Q1 is switched on, C_2 is charged through R_5, giving the front of the waveform. When the voltages on C_1 and C_2 are equal, these capacitors will discharge though R_8, R_{10} and R_{11} giving the exponential tail of the wave. When the transistor Q2 is switched on, this produces a rapid 'chop' of the voltage by discharging C_2 through R_6. Q2 is controlled by the variable output from the Philips generator thus allowing the chop delay and the fall time to be determined. Q3 acts as a buffer between the load (50 Ω) and the circuit output (C_2).

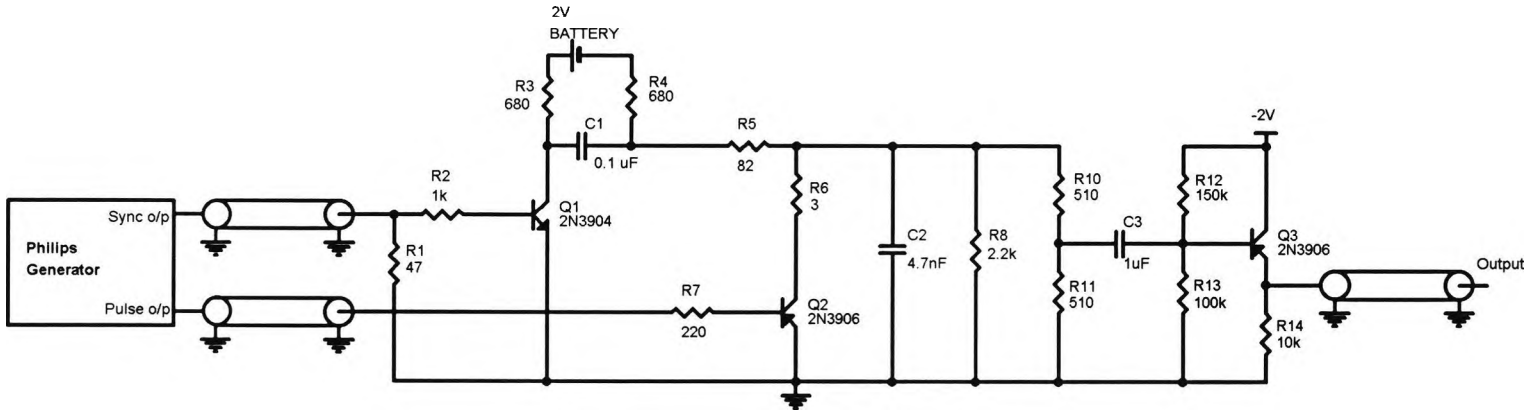


Fig. I.1 Chopped-Impulse Circuit Diagram

Appendix J Data Sheet For the RAM

VS12G476

Registered I/O,
Self-Timed, 1K x 4 Static RAM

Features

- 1024 by 4-bit static RAM for cache or control store applications
- Very fast Read/Write cycle time ..... 2.5 ns
- Single power supply (2 Volts)
- Completely static operation
- Very low sensitivity to total dose radiation
- 'Native' GaAs compatible inputs and outputs for ultra high speed interface
- Registered data inputs and outputs
- 28-pin leaded or leadless ceramic packages
- Fully decoded synchronous operation
- Low power dissipation ..... < 1 W Typ

Functional Description

The Vitesse VS12G476 is a very high speed, fully decoded synchronous 1024 x 4-bit read/write static random access memory. The VS12G476 is self-timed and all data inputs and outputs are registered. The product needs only a single 2 Volt power supply. It is compatible in ECL board environments between -2 and 0 Volts, or in GaAs circuit board environments between 0 and +2 Volts. Input and output signal levels are shifted accordingly.

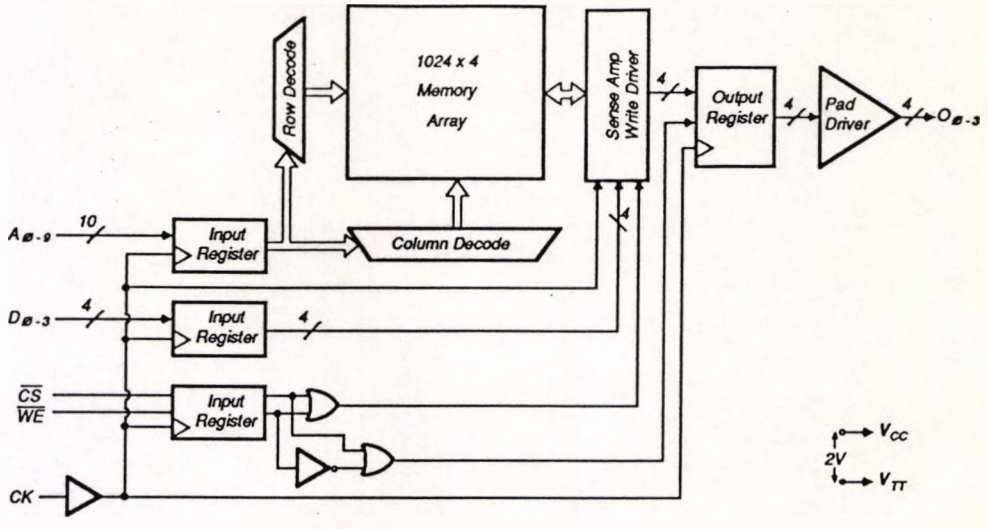
This product is designed to interface with other GaAs I/O products such as the FURY Series of gate arrays for ultra high speed chip to chip communication. The inputs and outputs of the VS12G476 utilize I/O levels which are 'native' to E/D GaAs technology and are consistent with 50 transmission line circuit board environments.

Memory cell selection is achieved through a 10-bit address designated A_0 - A_9. The address inputs, as well as the four data inputs, chip select and write enable are registered and held at the rising edge of the clock input. During a read, data out is valid after the clock access time (t_{CO}), and is registered and held into the next clock cycle, until the data change for the read cycle. During a write, data out is not driven. Data outputs are open source followers which provide maximum flexibility in a wired-OR application. The minimum cycle time for a read or write is 2.5 ns.

The VS12G476 is packaged in a 28-pin ceramic LDCC or LCC. Its high speed makes it ideal for new designs in cache memory, signal processing, and video applications where access time is the critical parameter. Its low sensitvity to total dose radiation makes it well-suited to the harsh environments encountered in military and aerospace applications.

The VS12G476 is fabricated in gallium arsenide using Vitesse's proprietary enhancement/depletion mode technology for high speed, low power operation.

Block Diagram



Truth Table

Inputs			
$\overline{CS}$	$\overline{WE}$	Output	Mode
H	X	L	Chip not selected, Output disabled
L	H	Data Out	Read
L	L	L	Write, Output disabled

H = HIGH Voltage L = LOW Voltage X = Don't Care (HIGH or LOW)

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT} = GND [V_{CC} - V_{TT}]) (2) ..... 4.0 V to -0.5 V
Power Supply Voltage (V_{CC} = GND [V_{TT} - V_{CC}]) (3) ..... -4.0 V to 0.5 V
Input Voltage Applied, (V_{TT} = GND) (2) ..... -0.5 V to V_{CC} + 0.5 V
Input Voltage Applied, (V_{CC} = GND) (3) ..... 0.5 V to V_{TT} - 0.5 V
Output Current, (I_{OUT}) ..... 30 mA
Maximum Junction Temperature, (T_J) ..... 150 C
Case Temperature Under Bias, (T_C) ..... -55 to +125 C
Storage Temperature, (T_{STG}) (4) ..... -65 to +150 C

Recommended Operating Conditions

Power Supply Voltage (V_{TT} = GND) (2) ..... 2.2 V to 1.8 V
Power Supply Voltage (V_{CC} = GND) (3) ..... -2.2 V to -1.8 V
Operating Temperature Range (4) ..... 0 to +70 C

Notes: *(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
(2) For operation in a +2 V GaAs circuit board environment.
(3) For operation in a -2 V ECL circuit board environment.
(4) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC Characteristics

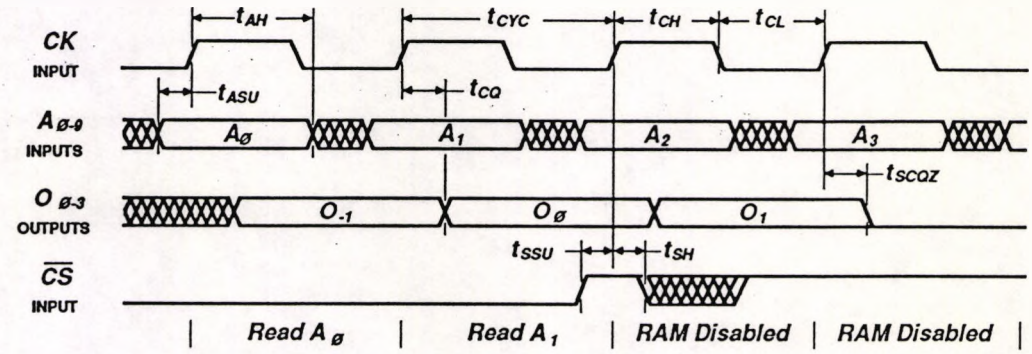
(Over recommended operating conditions Outputs terminated to V_{TT} through 50 .)

Parameters	Description	Min	Max	Units
V_{OH}	Output HIGH voltage	V_{TT} + 700	V_{TT} + 1100	mV
V_{OL}	Output LOW voltage	V_{TT}	V_{TT} + 100	mV
V_{IH}	Input HIGH voltage	V_{TT} + 600	V_{TT} + 1200	mV
V_{IL}	Input LOW voltage	V_{TT} - 400	V_{TT} + 200	mV
I_{TT} , I_{CC} (1)	Power supply current		500	mA

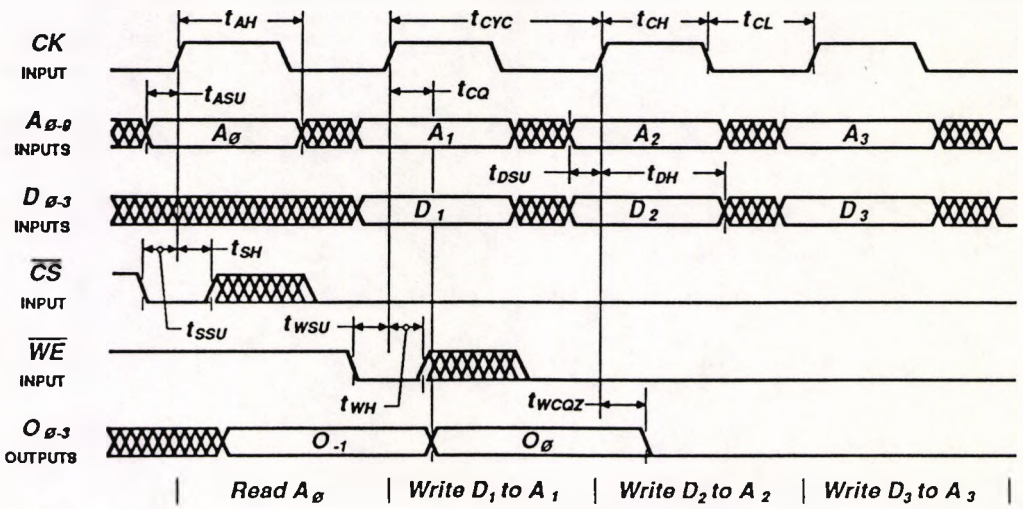
AC Characteristics(2)

(Over recommended operating conditions; Outputs terminated to V_{TT} through 50 .)

1. Read Mode:



2. Write Mode:



= DON'T CARE

NOTES: (1) The power supply can be configured in two ways: a) V_{CC} = 0 V (GND), V_{TT} = -2 V, or b) V_{CC} = +2 V, V_{TT} = 0 V (GND).

(2) Input edge rates are 500 ps or less. Timing is referenced to V_{TT} + 400 mV on inputs and outputs. Outputs terminated to 50 to V_{TT} and loaded by 30 pF.

AC Characteristics (continued) (1)

(Over recommended operating conditions; Outputs terminated to V_{TT} through 50 ohms.)

Parameters	Description	Min	Max	Units
t_{ASU}	Address setup time	—	0.7	ns
t_{DSU}	Data in setup time	—	0.7	ns
t_{SSU}	$\overline{CS}$ setup time	—	0.7	ns
t_{WSU}	$\overline{WE}$ setup time	—	0.7	ns
t_{AH}	Address hold time	0	—	ns
t_{DH}	Data hold time	0	—	ns
t_{SH}	$\overline{CS}$ hold time	0	—	ns
t_{WH}	$\overline{WE}$ hold time	0	—	ns
t_{CQ}	Clock to output	0	1.0	ns
t_{CYC}	Clock cycle time (read, write)	2.5	—	ns
t_{CH}	Clock HIGH time	1.0	—	ns
t_{CL}	Clock LOW time	1.0	—	ns
t_{SCQZ}	Clock to output disable (result of rising $\overline{CS}$ input)	—	1.0	ns
t_{WCQZ}	Clock to output disable (result of falling $\overline{WE}$ input)	—	1.0	ns

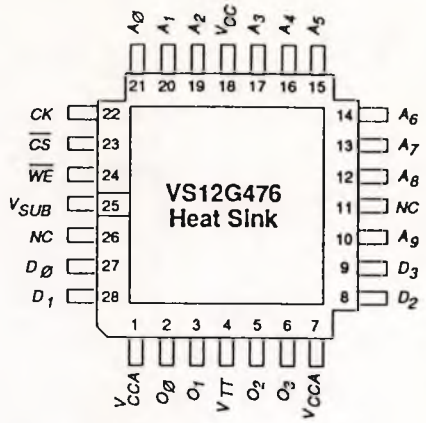
NOTES: (1) Input edge rates are 500 ps or less. Timing is referenced to V_{TT} + 400 mV on inputs and outputs. Outputs terminated to 50 to V_{TT} and loaded by 30 pF.

Pin Description

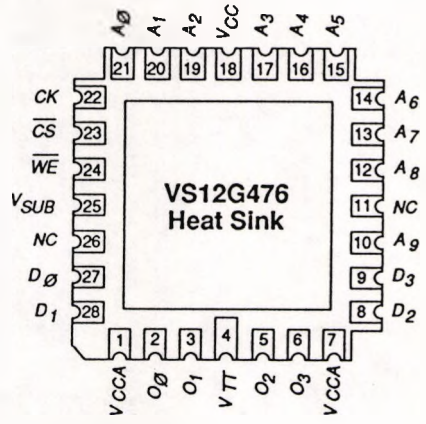
Pin #	Name	I/O	Description
10, 12-17, 19-21	A_0 - A_8	I	Address inputs
8, 9, 27, 28	D_0 - D_3	I	Data inputs
23	$\overline{CS}$	I	Chip select input (active LOW)
24	$\overline{WE}$	I	Write enable input (active LOW)
22	CK	I	Clock input
2, 3, 5, 6	$\overline{O_0}$ - $\overline{O_3}$	O	Data outputs
18	VCC		Most positive power supply voltage (1)
4	VTT		Most negative power supply voltage (2)
25	VSUB		Substrate voltage, connect to V_{TT}
1, 7	VCCA		Output driver supply voltage
26, 11	NC		No connect, leave floating

NOTES: (1) V_{CC} = 0 V in ECL environments; +2 V in GaAs environments.
(2) V_{TT} = -2 V in ECL environments; 0 V in GaAs environments.

Connection Diagram (28-pin LCC - Top View)



Connection Diagram (28-pin LDCC - Top View)



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