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# High performance low voltage operated organic field-effect transistors with low pinch-off voltages**

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**Abstract:** Organic field-effect transistors suffered ultra high operating voltage besides their relative low mobility. A general approach to low voltage operated organic field-effect transistors (OFETs) using donor/acceptor buffer layers is demonstrated. P-type OFETs with acceptor molecule buffer layers show reduced operating voltages (from 60–100 V to 10–20 V), with mobility up to 0.19 $cm^2/Vs$ and an on/off ratio of $3 \times 10^6$. The subthreshold slopes of the devices are greatly reduced from 5–12 V/decade to 1.68–3 V/decade. This favorable combination of properties means that such OFETs can be operated successfully at voltages below 20 V ($|V_{DS}| \leq 20$ V, $|V_{GS}| \leq 20$ V). This method also works for n-type semiconductors. The reduced operating voltage and low pinch-off voltage attribute to improved ordering of polycrystalline films, reduced grain boundary resistance and steeper subthreshold slopes.

Organic field-effect transistors (OFETs) have received tremendous attentions in the field of flexible and printable electronics.[1] A severe limitation for the development and realistic applications of organic electronics is the high operating voltage of OFETs (due to large band gap of organic semiconductors), about tens or up to 60–100 V.[2] The operating voltage is too high even for high-mobility materials such as pentacene or rubrene, whose mobility (on the order of 1 $cm^2/Vs$) and on/off ratio ($10^6$) are similar to the ones reported for hydrogenated amorphous silicon (α-Si:H) devices.[3,4] This shortcoming can be demonstrated by comparing the subthreshold slopes of α-Si:H devices (about 0.5 V/decade) and those of pentacene based OFETs, which are about 5–12 V/decade or higher.[5] Low-voltage operation ($|V_{DS}| \leq 20$ V, $|V_{GS}| \leq 20$ V) will contribute to cost savings by enabling the use of lower cost driver electronics, making OFETs particularly suitable for most rapidly growing portable applications, e.g., in electronic papers and Radio Frequency Identification (RFID) tags.[6,7]

The large threshold voltage and large subthreshold slope (typically > 5 V/decade) of OFETs make application in low-voltage circuits problematic. To overcome this critical issue, researchers try to use very thin,[8] monolayer dielectric layers[7] or high-*k* gate materials[9,10] which allow the necessary high capacitance to accumulate charge at much lower voltages. High capacitance means that high charge-carrier concentration can be reached at low gate voltage. However, the pinhole would be the major problem when reducing the dielectric thickness. Very thin or high-*k* gate dielectrics generally may bring about high leakage current and low dielectric strength

in the utilization of OFETs.[11] Another disadvantage of high-*k* gate dielectrics is the energetic disorder due to the changed localized states that induce carrier localization and reduce charge-carrier mobility due to high dipolar disorder at the interface.[12]

All these attempts have been focused on the capacitance of the dielectric layer, the general approach to low voltage operated OFETs and its mechanism should be explored. For example, high operating voltage of OFETs mainly origins from their high threshold voltages and high pinch-off voltages. Besides, OFETs with high capacitance dielectrics can not withstand a high voltage applied at the same time when they can be operated in a narrow range of voltage. It can be more serious when both low and high operating voltage devices are required in integrated organic circuits especially when amplificatory function (low operating voltage) and power electronic applications (high operating voltage) will be needed in the same circumstance.[13] Herein, we demonstrate a simple, universal and effective way of reducing the operating voltage of thin film OFETs ($|V_{DS}| \leq 20$ V, $|V_{GS}| \leq 20$ V) by introducing donor/accepter molecule buffer layers on thick thermal silicon oxide (about 500 nm) as gate insulator.

Pentacene, copper-phthalocyanine and perfluorinated copper-phthalocyanine (Fig. 1a, compound **1**, **2a** and **2b**) for example are widely used as semiconductors to build OFETs. But their operating voltages are extremely high (60–100 V, Fig. 2a). Although pentacene got high mobility up to 3–5 $cm^2/Vs$, its low voltage operation usually afforded poor modulations and with linear I–V curves with low on/off ratio (Fig. 2b) or nonohmic behavior (Fig. 2c). Devices using tetracyanoethylene (TCNE) acceptor

buffer layers exhibit very reproducible I–V characteristics at very low biases (10–20 V) with ideal linear and saturation response (Fig. 2d). The mobility of pentacene OFETs with 3 nm TCNE buffer layer was around 0.11–0.19 $cm^2/Vs$ with a threshold voltage of –8.1 V and a subthreshold slope of 1.68 V/decade at low drain-source voltage (Fig. 2e and 2f). This combination of favorable properties demonstrates that OFETs can be operated successfully at voltages below 20 V ($|V_{DS}| \leq 20$ V, $|V_{GS}| \leq 20$ V). In marked contrast, control devices fabricated without buffer layer on $SiO_2$ dielectric required far larger operating voltages (60–100V) for I–V characteristics with both apparent linear region and saturations (Fig. 2a). Note that our results were obtained using very thick $SiO_2$ dielectric (about 500 nm), neither high-*k* dielectric nor ultra thin insulator layer was used. To validate the universality of this approach and elucidate structure-function relationships, OFETs with buffer layers (Fig. 1b) using varied acceptor molecules with different numbers of cyano groups (Fig. 1a, compound **3a**, **3b**, **4a** and **4b**) were fabricated. Their low voltage performances were also impressive as shown in Fig. 3a ~ Fig. 3c and the device parameters were summarized in Table 1. The pinch-off voltage $V_{PO}$, which can be experimentally determined by the drain voltage intersection point of two extrapolated straight lines in the linear and the saturation regions of the $I_{DS}$–$V_{DS}$ output characteristics (as shown in the inserted drawing of Fig. 3d), decreased as the numbers of cyano-groups in the acceptor molecules were increased as shown in Fig. 3d.

The mobility of TCNE/pentacene OFET at low voltages (0.11–0.19 $cm^2/Vs$) was higher than those in linear region (within 20 V) of OFETs without TCNE acceptor

buffer layers (0.024–0.046 $cm^2$/Vs, Table 1). It has been reported that the transport properties of pentacene thin film transistors are determined by morphology of dielectrics and the interfaces between the pentacene and the dielectrics.[14] Surface morphology can have a significant influence on the mobility as well as on the subthreshold behaviors of thin film transistors. Figure 4a and 4c show the AFM images of pentacene grains on $SiO_2$ and TCNE/$SiO_2$. The pentacene film on the TCNE/$SiO_2$ layer (Fig. 4c) apparently had significantly larger grain size as compared to a similar film on the $SiO_2$ layer (Fig. 4a). To determine the molecular orientations of the films, XRD spectrums were measured with respect to out-of-plane structures. Typical out-of-plane XRD patterns of the vacuum-deposited films are shown in Fig. 4d. Both patterns showed strong peaks assigned to (*00l*) plane, which indicate the alignment of the long axis of pentacene molecules perpendicular to the substrate. Pentacene film on TCNE/$SiO_2$ showed, so called, “thin-film phase” with 15.4 Å of d spacing, while pentacene film on bare $SiO_2$ showed two separated d spacings of “thin-film phase” with 15.4 Å and “bulkphase” with 14.5 Å of d spacing as reported by many researches.[15,16] The charge carrier mobility of the bulk phase is evidentially lower than the mobility of the thin film phase.[17] It has also been reported that for pentacene films having mixed thin-film and bulk phases, mobilities were relative low, possibly due to the high defect densities arising from the coexistence of two phases.[18]

To explain the low pinch off voltages, we should consider I–V characteristics of OFETs at low voltages. In an FET, the charges are confined near the interface

between the molecular layer and the dielectric, because of the strong electric field used to inject the charges. The drain current saturated when the charges in the accumulation channel around the drain electrode was depleted by the electric field of the drain electrode. If saturated drain current is to be obtained, the interface barrier between the metal electrode and the semiconductor layer should be sufficiently reduced to produce a large injection of charges described by the Fowler-Nordheim Equation,[19] which strongly depends on the electric field at the interface. It has been reported that the contact resistance becomes increasingly important when the length of the channel is reduced and the transistor operates at low fields. The electric field has to exceed a critical value to obtain a saturated drain current. The charge injection from the source to form the channel could be aided by selective doping of the semiconductor under the contacts and at the semiconductor/dielectric interface.[20,21] We believe that interactions between pentacene and TCNE influenced the charge carrier density and the transport properties at low drain-source voltages, inducing the ideal ohmic behavior in output OFET characteristics.

Generally, low operating voltage requires at first a low threshold voltage of only a few volts and steep sub-threshold slope. The subthreshold slope determines the voltage swing required for a transistor to turn from “off” to “on”, and should be as low as possible. A high subthreshold slope is a traditional weakness of organic transistors that results from their low gate-dielectric capacitance, which reduces swing speed. The threshold voltage $V_T$ can be written as the sum of two contributions,[22]

$$V_T = V_{SC} + V_{FL} \quad (1)$$

$V_{FL}$ is the flat level potential that accounts for any work function difference between the organic film and the gate, and for any physical or chemical interface dipole moment or trapped charge at the gate/oxide and oxide/organic interfaces, and $V_{SC}$ is the voltage drop across the organic semiconductor. Although both $V_{SC}$ and $V_{FL}$ take important roles in the reduction of the operating voltage of OFETs, in our opinion it's not the whole story. For example, although $V_T$ has been claimed could be controlled in a wide range by different methods, they did not produce low voltage operated OFETs although $V_T$ was well controlled very close to 0 V in some cases. [23–25]

For the output characteristics, once the saturation region is reached, the increase in drain voltage does not cause increase in current. A pinch off region is observed followed by a saturation level as the drain voltage increases. The pinch-off point $V_{PO}$ can be calculated through Equation 2,[22]

$$V_P = -\frac{qNd_s^2}{2\varepsilon_s}\left(1+2\frac{C_s}{C_i}\right)+V_{FL} \approx -\frac{qNd_s}{C_i}+V_{FL} \quad (2)$$

where $N$ is the doping level, $d_s$ the thickness of the semiconducting film, $C_s$ and $C_i$ are the capacitance of the semiconductor and the dielectric. This equation was derived directly from the theory of the metal-semiconductor FET by assuming that the doping level in organic semiconductors was very low.[22] Generally, pinch-off point $V_{PO}$ could be reduced by increasing the dielectric capacitance, or by reducing the doping level and $V_{FL}$. But our extrapolations based on the Equation 2 did not match our experimental results, partly because our channels were selectively doped with donor and acceptor molecules, so the mechanism of our low pinch off voltage OFETs should be re-explored.

We consider that TCNE layer not only changed the film morphology but also had strong effects on the electrical properties of grain boundaries. It has been recognized quite early that the localization of electrons and/or holes (also referred to as traps) influence in a direct way the transport of the carriers. An important parameter characterizing traps is their depth. In disordered solids the trap depth may be defined as the energy necessary to excite a carrier from a local state to a transport level. When pentacene and TCNE are brought together into contact, energy bands will experience a bending, the highest occupied molecular orbital (HOMO) of pentacene being bent upwards and the lowest unoccupied molecular orbital (LUMO) of TCNE being bent downwards. This situation favors a charge transfer between pentacene and TCNE, which results in the accumulation of charge carriers, electrons in TCNE and holes in pentacene, at both sides of the interface, and, in turn, in a build-in electrical field, leading to the formation of a polarized layer and an interface dipole at the interface between pentacene and TCNE.[26,27]

The infrared ray (IR) featureless absorptions in the region 2350–2000 $cm^{-1}$ are analyzed for the nature of charge transfer transitions between TCNE and pentacene as shown in Fig. 5a. TCNE complexes shows a larger gap ($Eg$ = 0.27 eV) compared to tetracyanoquinomethane (TCNQ), dichloro dicyano quinone (DDQ) complexes. This indicates that the TCNE complex is Mott or Hubbard semiconductor rather than a Peireels semiconductor.[28] Due to the charge transfer effect, it is electrochemically easy to transfer an electron, reversibly, from the donor to TCNE to form $TCNE^{\bullet/-}$, a stabilized and persistent radical anion.[29] Thus, the radical anion will greatly enhance

the carrier mobility,[30] resulting in relative low pinch off voltage devices which can be operated using low voltages within 20 V.

Another fact should be noted is that our pentacene grains were formed on high density uncontinous nano sized TCNE islands on the $SiO_2$ layer as shown in Fig. 4b. The field-effect mobility is dominated by the mobility in grain boundaries, because the mobility of the grain boundaries is generally much smaller than the bulk semiconductor inside the grain. The effective mobility $u_{effective}$ in polycrystalline materials is given by,[31]

$$\frac{1}{u_{effective}} = \frac{1}{u_S} + \frac{1}{u_G} \tag{3}$$

where $u_S$ is the bulk mobility of semiconductor (inside the grain) and $u_G$ the grain boundary mobility, which is generally given by thermionic emission over the barrier. We found that charge transfer complexes formed between the TCNE and organic semiconductors greatly reduced the grain boundary resistance. This conclusion is supported by the fact that the slightly improved conductance of the films at zero gate voltage was observed for pentacene/TCNE based transistors as shown in Fig. 5b. The conductivity of the channel with 3 nm TCNE was about 20 times higher than that of the pure pentacene film.

At pinch-off voltage, a depletion region starts to form around the electrode as the charges density approaches zero, and reaches zero at saturation. When $V_{DS} = V_G - V_T$, a point with no gate-induced charge is created near the drain, the so-called “pinch-off point.” When $V_{DS}$ exceeds $V_G - V_T$, the pinch-off point shifts towards the source, and a pinch-off region is formed between the drain and the pinch-off point. At any $V_{DS}$

larger than $V_{PO}$, the potential between the source and the pinch-off point is $V_{PO}$, and the excess potential $V_{DS} - V_{PO}$ drops across the pinch-off region. Consequently, when $V_{DS}$ increases, the pinch-off region extends slightly. In our selected doped film configurations, the differential resistance in the saturation region is lower due to the reduced grain boundary resistance and the more preferable mobile carriers induced by the gate voltage. Since there is no hole accumulation in the pinch-off region (note that our acceptor doping is discontinuous), its resistance is very high compared to the channels induced by the gate voltage.[32] As a result, the constant potential drop on the undepleted channel will be reduced, resulting in a lower $V_{PO}$ than their undoped counterpoints. In other words, the acceptor layers changed the potential profile along the channel length orientation. On the contrary, conventional doping methods greatly enhanced the carrier density in the whole channel thus degenerated the modulations of the devices.[33,34] The increased carrier density, however, will make it impossible for pinch-off region to be fully depleted,[35] which will enhance the operating voltage of OFETs and degrade the device performances.

To ensure the effectiveness and adaptivity of our method of reducing the operating voltage, one major challenge is if it works for low mobility semiconductors. CuPc, for example, is an ideal material for OFETs due to its superior stability, but its mobility is relative low. We fabricated the low operating voltage OFETs with TCNE (3 nm)/CuPc (50 nm) as active layers. The devices showed typical transistor performance within 20 V for both drain and gate voltages (Fig. 6a and 6b). Similar transistor characteristics are obtained using a range of organic semiconductors such as

NiPc, ZnPc and $F_{16}$CoPc with relative low mobility, demonstrating broad generality.

Although acceptors such as TCNE are also effective in reducing the operating voltage for n-type materials, the electron mobility was not high as shown in Table 1. In our opinion, the mismatch of the energy level between TCNE and $F_{16}$CuPc caused electron traps with high trap depth. So we tried to use bis(ethylenedithio) tetrathiafulvalene (BEDT-TTF) as the buffer layers for n-type OFETs. OFETs with 3 nm BEDT-TTF got impressively low $V_{PO}$, as shown in Fig. 7b and 7c. The devices afforded a mobility of $5.2 \times 10^{-4}$ $cm^2/Vs$ with current on/off ratio up to $1.5 \times 10^5$ and a threshold voltage of about +1.7 V (Fig. 7d), much better than that of n-type OFETs with acceptor buffer layers or on bare $SiO_2$ (Fig. 7a). We further fabricated invertors using low voltage operated OFETs with TCNE/pentacene and BEDT-TTF/$F_{16}$CuPc, the gain at $V_{DD} = -20$ V and $-100$ V voltages were about 3.2 and 6.7, respectively. Relative low gain was due to the limited mobility of n-type semiconductor we utilized. Despite that, our method demonstrated here implies that a novel, universal approach to low voltage OFETs has been realized.

In conclusion, a novel methodology for fabricating low operating voltage OFETs ($|V_{DS}| \leq 20$ V, $|V_{GS}| \leq 20$ V) based on donor/acceptor molecules has been demonstrated. This technique is compatible with existing silicon and OFET process, and the resulting devices function at low voltages with a variety of semiconductors, suggesting a new route to low power consumption organic electronics.

***Experimental***

All compounds were obtained from Aldrich Chemical and were purified by temperature-gradient vacuum sublimation. Highly doped Si-wafers with 500 nm thermally oxidized $SiO_2$ dielectric are used as a substrate. Prior to the active-layer deposition, a thin layer of acceptor/donor molecules were deposited at a deposition rate near 0.1 Å/s. The thickness of the buffer layer was controlled by a quartz crystal film thickness monitor. Organic semiconductors (pentacene, CuPc, $F_{16}$CuPc, etc) were then deposited by thermal evaporation onto substrates held at room temperature with a deposition rate near 0.5 Å/s. Gold source and drain electrodes were then made through shadow mask using thermal evaporation. The defined channel width (W) and length (L) were 3000 μm and 50 μm, respectively.

We mainly studied four groups of devices, p-type with donors, p-type with acceptors, n-type with donors and n-type with acceptors. We used pentacene and CuPc as p-type semiconductors, and $F_{16}$CuPc as n-type material. Compound **3a**, **3b**, **4a** and **4b** were selected as acceptors as they showed proper acceptor ability. Bis(ethylenedithio) tetrathiafulvalene (BEDT-TTF) was used as donor molecule for control experiment. OFETs with p-type with donors showed degenerated performances. If strong donors such as dibenzotetrathiafulvalene (DBTTF), or acceptors such as TCNQ were used, strong charge transfer effect occurred and the device performance got serious degenerations.

The OFETs were characterized with Hewlett-Packard (HP) 4140B semiconductor parameter analyzer at room temperature. AFM images were obtained using a Digital

Instruments nanoprobe atomic force microscopic (AFM) in the tapping mode. X-ray diffraction (XRD) measurements were carried out in the reflection mode at room temperature using a 2-kW Rigaku X-ray diffraction system (Cu Kα radiation, λ = 1.54 Å). Infrared Ray spectra were determined using a BRUKER TENSOR 27 spectrometer.

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## Figure Legends

**Figure 1.** Chemical structure of (a) pentacene (**1**), copper phthalocyanine (**2a**, CuPc) and perfluorinated copper phthalocyanine (**2b**, $F_{16}$CuPc), tetracyanoethylene (**3a**, TCNE), 2,3-diaminomaleonitrile (**3b**), benzene-1,2,4,5-tetracarbonitrile (**4a**) and phthalonitrile (**4b**). (b) Schematic drawing of the proposed OFET structure.

**Figure 2.** Output characteristics of a pentacene (50 nm) OFET fabricated on 500 nm $SiO_2$ with $V_{DS}$ (a) within –100 V, (b) in the small bias range. (c) Output characteristics of OFET with high contact resistance. (d) Output characteristics of an OFET based on TCNE (3 nm)/pentacene (50 nm) at its transfer characteristics at (e) $V_{DS}$ = –20 V, (f) $V_{DS}$ = –100 V. The channel length is 50 μm and the width is 3000 μm.

**Figure 3.** Output characteristics of pentacene OFETs with 3 nm compound (a) **3b**, (b) **4a**, and (c) **4b**. (d) Dependence of the pinch off voltage on the thickness of acceptor molecule buffer layers, inserted is the schematic drawing of extracting the pinch-off voltage $V_{PO}$.

**Figure 4.** AFM images of (a) pentacene (b) TCNE, (c) TCNE (3 nm)/pentacene (50 nm) on $SiO_2$ substrate. (d) XRD patterns for pentacene with and without TCNE.

**Figure 5.** (a) IR featureless absorptions of TCNE and pentacene in the region 2350–2000 $cm^{-1}$, (b) I–V characteristics of pentacene and TCNE/pentacene films at

zero gate voltage.

**Figure 6.** (a) Output and (b) transfer characteristics of an OFET based on TCNE (3 nm)/CuPc (50 nm).

**Figure 7.** (a) Output characteristics of an OFET based on $F_{16}$CuPc (50 nm) on 500 nm bare $SiO_2$. (b) BEDT-TTF (3 nm)/$F_{16}$CuPc (50 nm), low operating (c) output characteristics and (d) transfer characteristics at $V_{DS}$ = 20 V of the same device.

Figure 1.

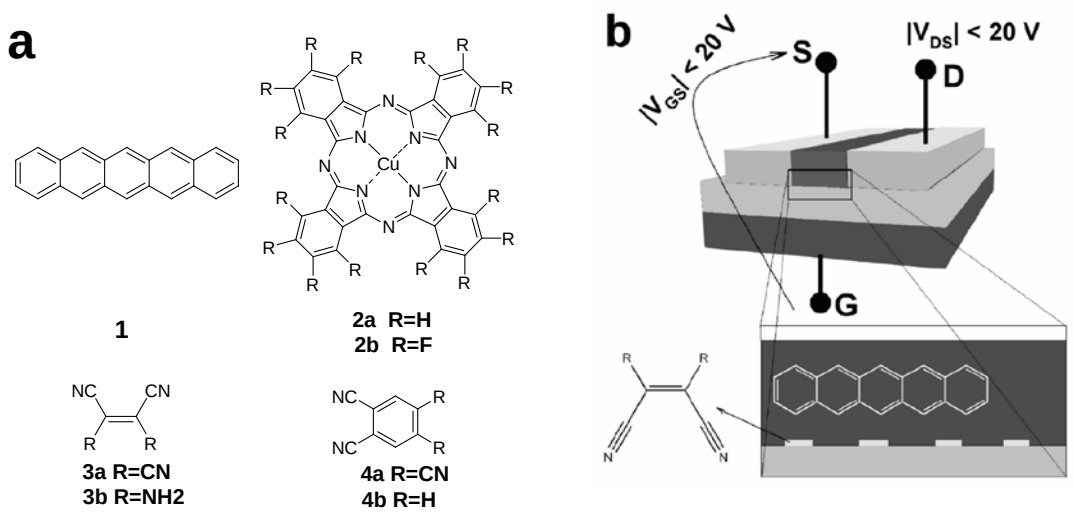
a
1
2a R=H
2b R=F
NC
CN
R
3a R=CN
3b R=NH2
4a R=CN
4b R=H
b
|V_GS| < 20 V
|V_DS| < 20 V
S
D
G

Figure 2.

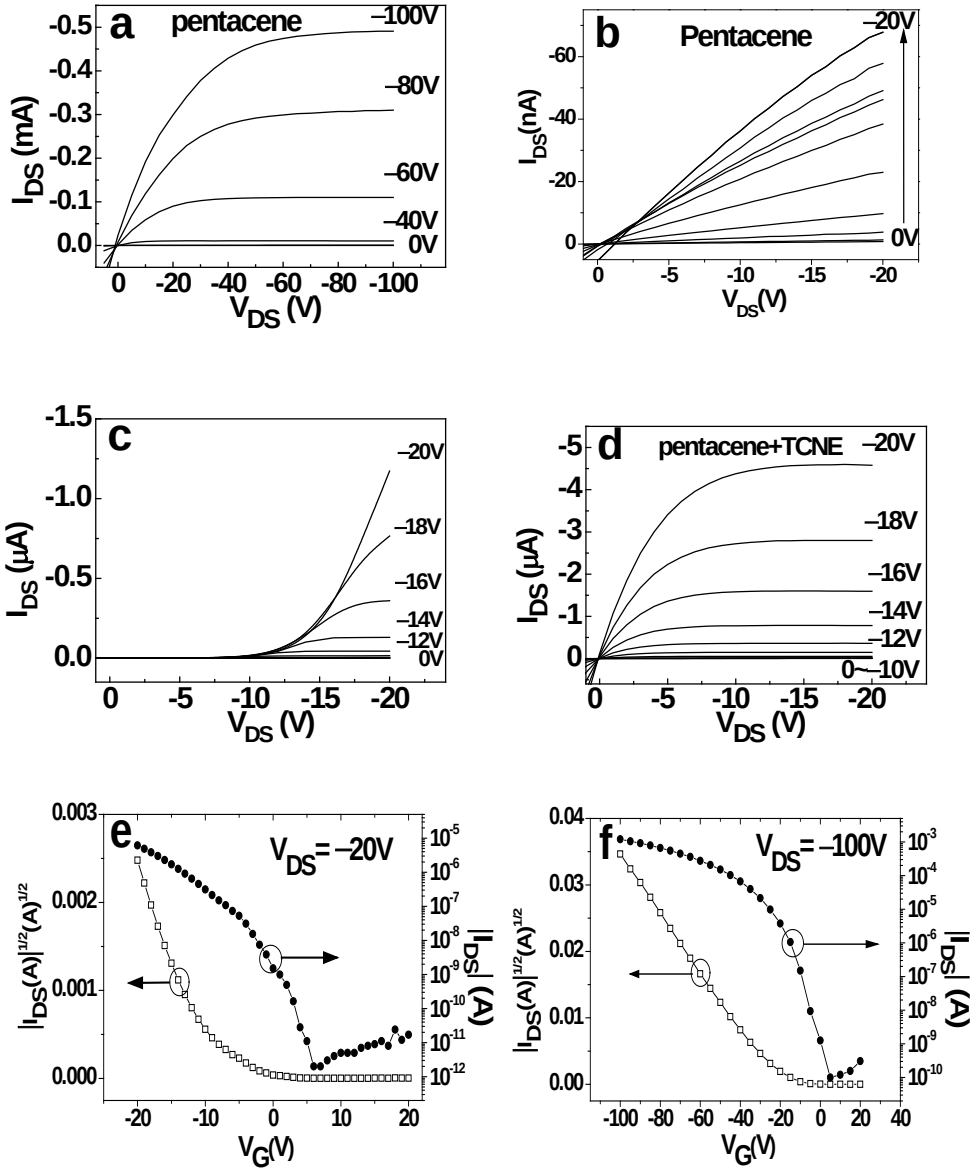
a
pentacene
–100V
–80V
–60V
–40V
0V
$I_{DS}$ (mA)
$V_{DS}$ (V)
b
Pentacene
–20V
0V
$I_{DS}$(nA)
$V_{DS}$(V)
c
–20V
–18V
–16V
–14V
–12V
0V
$I_{DS}$ (μA)
$V_{DS}$ (V)
d
pentacene+TCNE
–20V
–18V
–16V
–14V
–12V
0~–10V
$I_{DS}$ (μA)
$V_{DS}$ (V)
e
$V_{DS}$= –20V
$|I_{DS}(A)|^{1/2}(A)^{1/2}$
$|I_{DS}|$ (A)
$V_G$(V)
f
$V_{DS}$= –100V
$|I_{DS}(A)|^{1/2}(A)^{1/2}$
$|I_{DS}|$ (A)
$V_G$(V)

Figure 3.

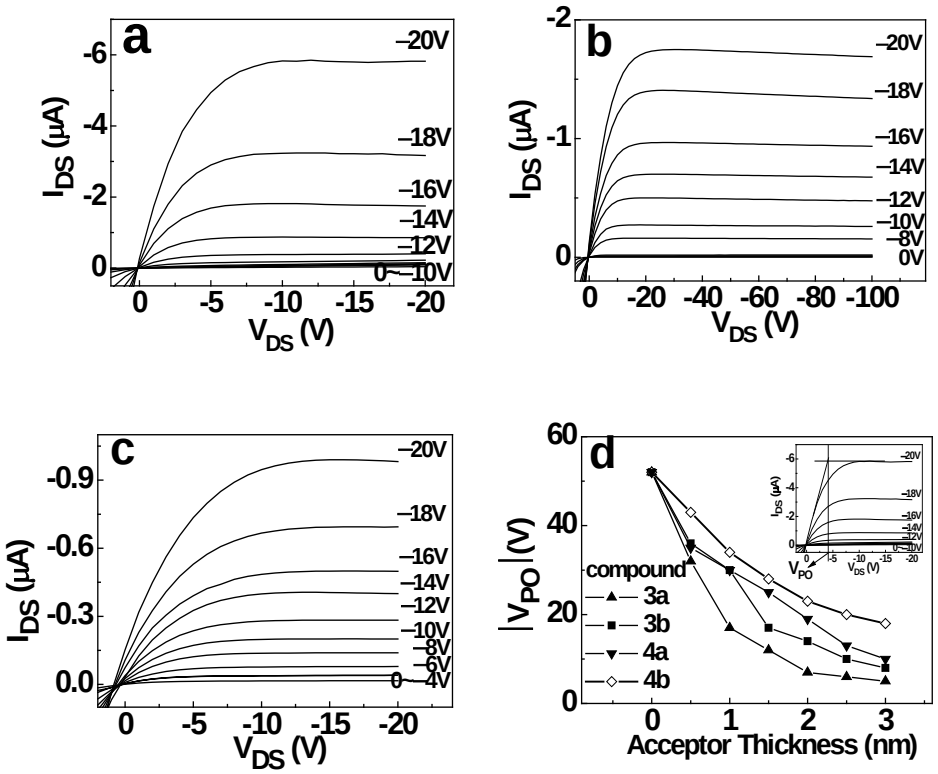
a
b
c
d
$I_{DS}$ (μA)
$V_{DS}$ (V)
–20V
–18V
–16V
–14V
–12V
–10V
–8V
–6V
–4V
0V
compound
3a
3b
4a
4b
$|V_{PO}|$ (V)
Acceptor Thickness (nm)

Figure 4

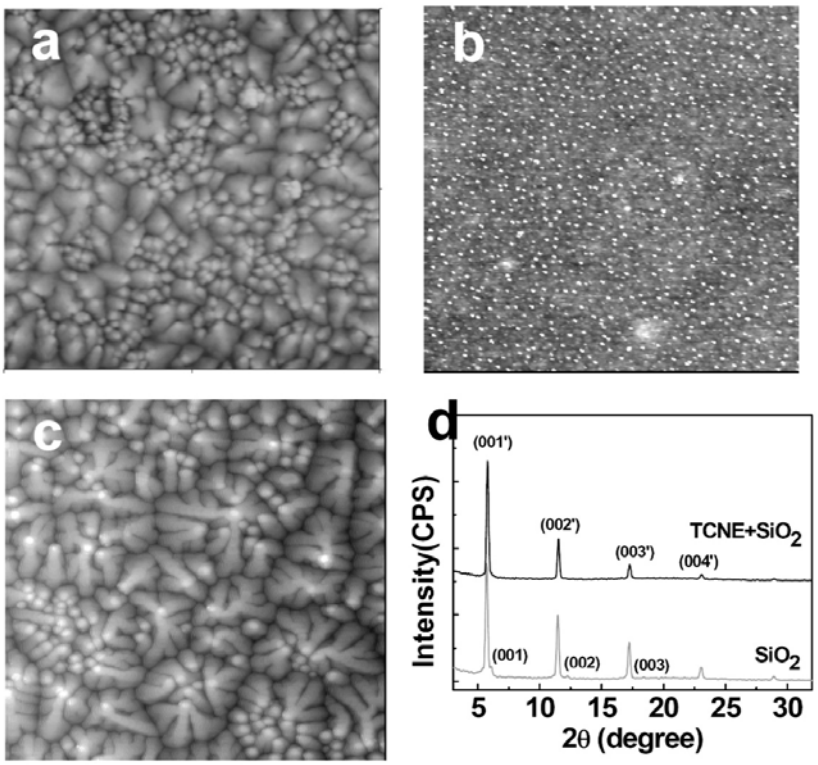
a
b
c
d
(001')
(002')
(003')
(004')
TCNE+SiO2
(001)
(002)
(003)
SiO2
Intensity(CPS)
5
10
15
20
25
30
2θ (degree)

Figure 5.

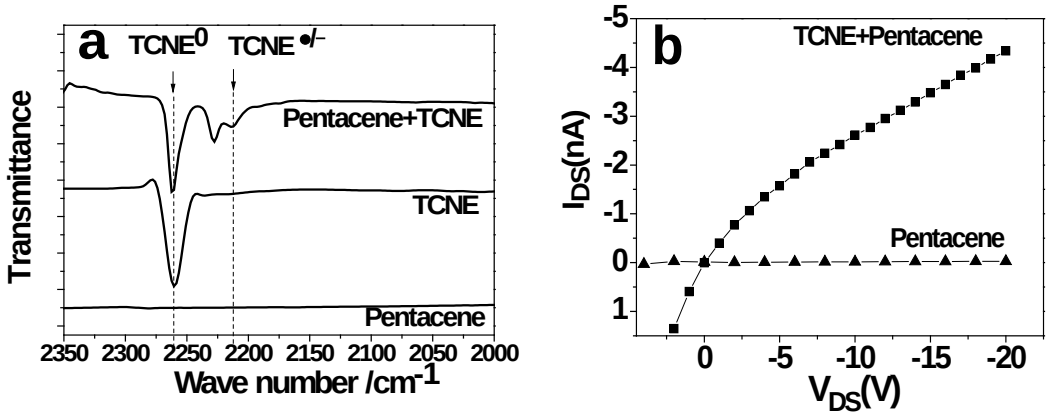
a
TCNE0
TCNE •/–
Pentacene+TCNE
TCNE
Pentacene
Transmittance
2350 2300 2250 2200 2150 2100 2050 2000
Wave number /cm-1
b
TCNE+Pentacene
Pentacene
IDS(nA)
-5 -4 -3 -2 -1 0 1
0 -5 -10 -15 -20
VDS(V)

Figure 6

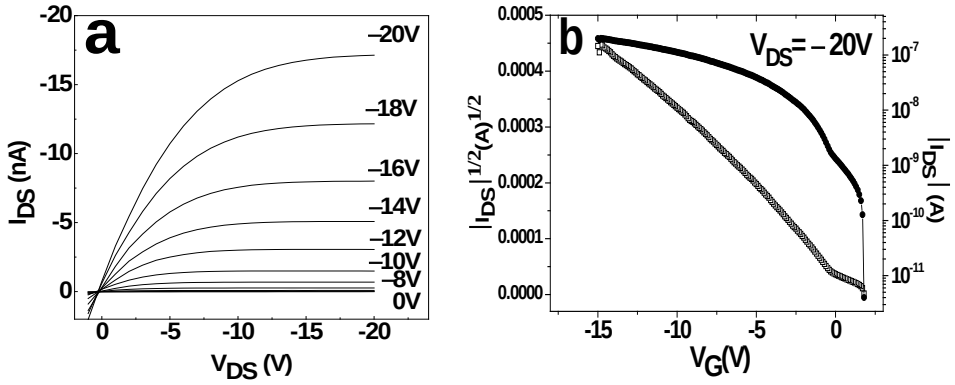
a
–20V
–18V
–16V
–14V
–12V
–10V
–8V
0V
I_DS (nA)
V_DS (V)
b
V_DS= – 20V
|I_DS|^1/2(A)^1/2
|I_DS| (A)
V_G(V)

Figure 7.

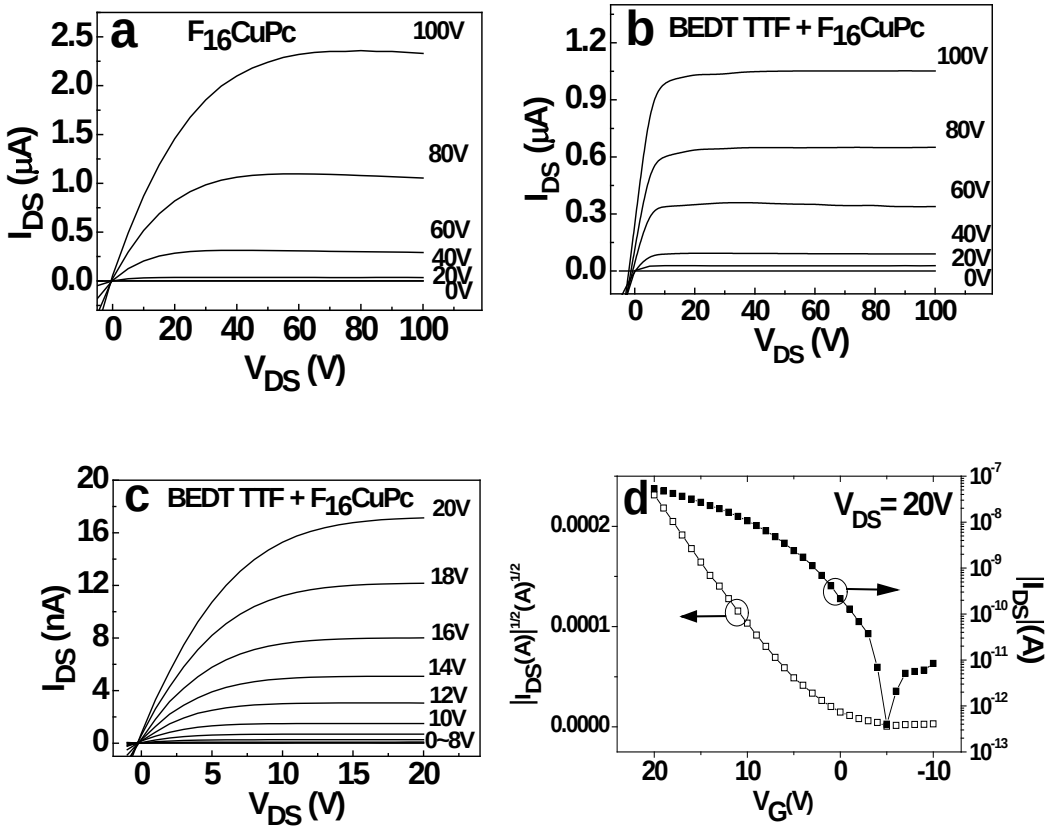
a
F16CuPc
100V
80V
60V
40V
20V
0V
IDS (μA)
VDS (V)
b
BEDT TTF + F16CuPc
100V
80V
60V
40V
20V
0V
IDS (μA)
VDS (V)
c
BEDT TTF + F16CuPc
20V
18V
16V
14V
12V
10V
0~8V
IDS (nA)
VDS (V)
d
VDS= 20V
|IDS(A)|1/2(A)1/2
|IDS|(A)
VG(V)

**Table 1. Device performance comparisons of OFETs with various acceptors.**

| | Pentacene | | $F_{16}CuPc$ | | Operating Voltages [V] |
|---|---|---|---|---|---|
| **Buffer layer** | **Mobility [$cm^2$/Vs]** | **$V_T$ [V]** | **Mobility [$cm^2$/Vs]** | **$V_T$ [V]** | |
| **none** | 0.12<br>0.024 [a] | –16 | $6.1\times10^{-4}$<br>$2.5\times10^{-4}$* | +6.3 | **60~100** |
| **OTS [b]** | 0.63<br>0.046 [a] | –20 | $4.6\times10^{-3}$<br>$6.9\times10^{-4}$* | +12 | **60~100** |
| **3a** | 0.19 | –8.1 | $1.4\times10^{-4}$ | +0.53 | **10~20** |
| **3b** | 0.13 | –7.2 | $3.7\times10^{-5}$ | +5.6 | **15~20** |
| **4a** | 0.083 | –2.9 | $2.4\times10^{-5}$ | +8.2 | **15~20** |
| **4b** | 0.066 | –5.6 | $8.2\times10^{-5}$ | +7.3 | **25~30** |

[a] mobility of the same device at low operating voltages (linear region)

[b] modified by n-Octadecyltrichlorosilane.

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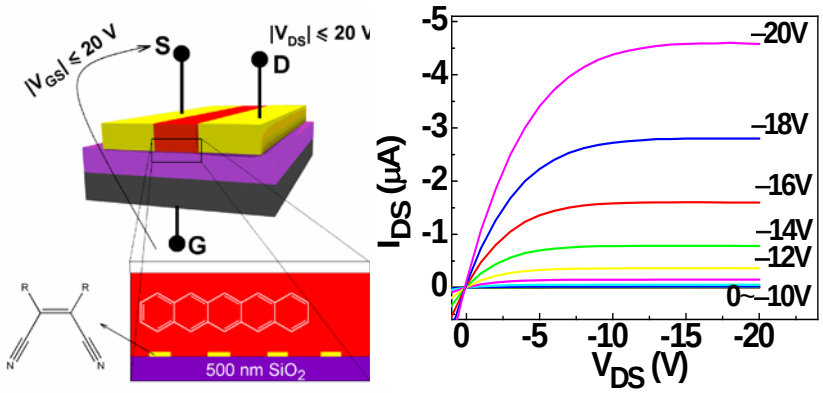
## High performance low voltage operated organic field-effect transistors with low pinch-off voltages

*By* Weiping Wu, Yunqi Liu*, Ying Wang, Hongxia Xi, Xike Gao, Chongan Di, Gui Yu, Wei Xu and Daoben Zhu




A general approach to low voltage operated organic field-effect transistors (OFETs) using donor/acceptor buffer layers is developed. P-type OFETs on 500 nm $SiO_2$ with acceptor molecule buffer layers show reduced operating voltages (from 60–100 V to 10–20 V), with mobility up to 0.19 $cm^2/Vs$, an on/off ratio of $3 \times 10^6$ and a subthreshold slope of 1.68 V/decade at low drain-source voltage.