A particle swarm optimization approach for designing III-V/Si vertical couplers

Rubio-Noriega, Ruth, Prosopio-Galarza, Roy, Oliveira, Luciano, Rahman, B. M. A., Hernandez-Figueroa, Hugo

Ruth E. Rubio-Noriega, Roy Prosopio-Galarza, Luciano P. Oliveira, B. M. A. Rahman, Hugo E. Hernandez-Figueroa, "A particle swarm optimization approach for designing III-V/Si vertical couplers," Proc. SPIE 11692, Optical Interconnects XXI, 116920T (5 March 2021); doi: 10.1117/12.2577995

SPIE.

Event: SPIE OPTO, 2021, Online Only

A particle swarm optimization approach for designing III-V/Si vertical couplers

Ruth E Rubio-Noriega[a], Roy Prosopio-Galarza[a], Luciano P. Oliveira[b], B.M.A. Rahman[c], and Hugo E. Hernandez-Figueroa[d]

[a]INICTEL, Universidad Nacional de Ingeniería, 1771 San Luis Ave., Lima, Peru
[b]Directed Energy Research Centre, Technology Innovation Institute, Abu Dhabi, United Arab Emirates
[c]School of Engineering and Mathematical Sciences, City University, EC1V 0HB London, U.K
[d]Communications Department, Universidade Estadual de Campinas, Cidade Universitaria Zeferino Vaz, Campinas, Brasil

ABSTRACT

III-V materials with quantum wells or quantum dot active regions have proven to be relatively efficient devices for amplifying light. However, integration and scaling of many other functions are moving towards the development of ever more complex photonic integrated circuits (PICs). Assembling these devices into hybrid/heterogeneous PICs poses a challenge in terms of bandwidth and footprint. In this work, we propose a Particle Swarm Optimized methodology to generate non-intuitive structures that couple light vertically from a III-V platform to a silicon-on-insulator chip. By designing heuristically optimized III-V and silicon tapers, we can overcome the limitations of typical linearly-varying spot-size converters in terms of footprint, without sacrificing bandwidth. Furthermore, the optimization parameters are adjusted to fit the usual design rule constraints that are ready for mass production, namely UV-lithography limits.

Keywords: spot-size converter, optical interconnects, hybrid silicon photonics

1. INTRODUCTION

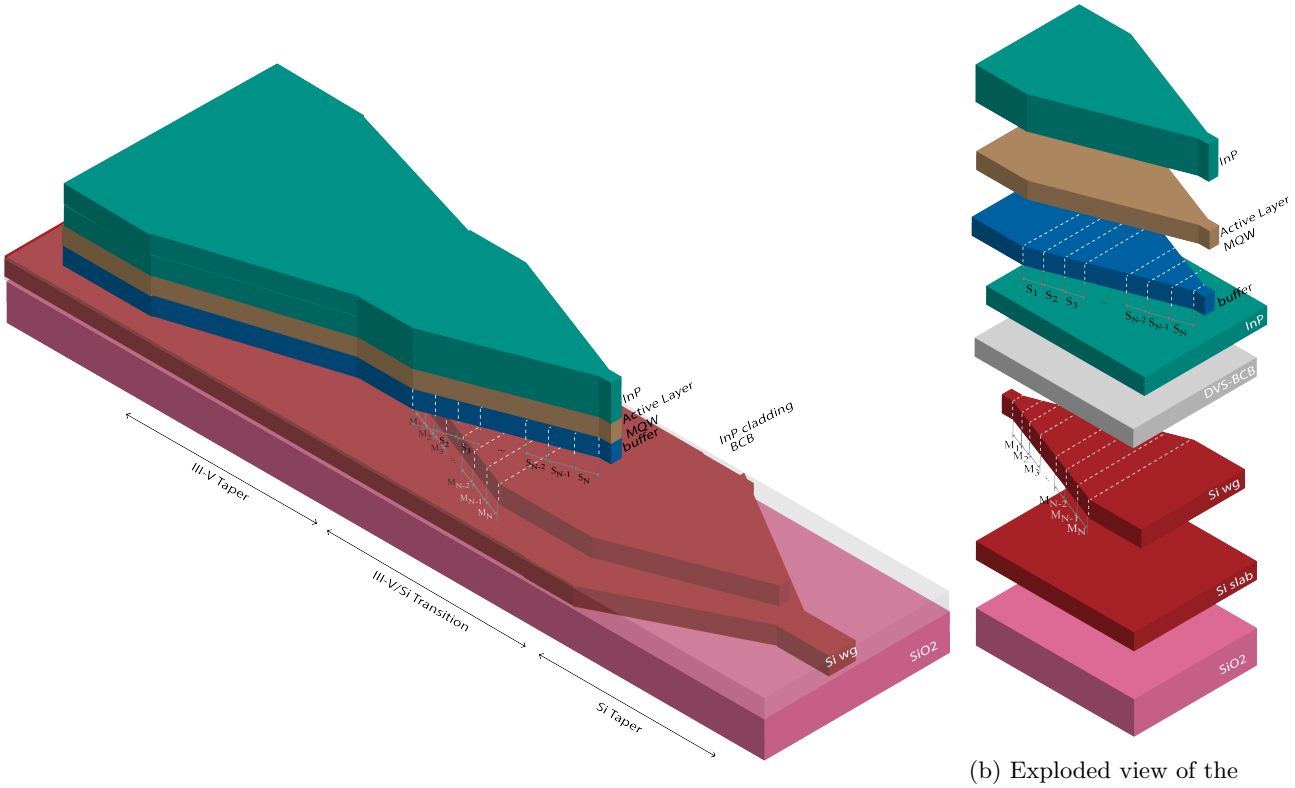
Large-scale integration of photonic integrated circuits (PIC) on silicon introduces the concept of hybrid integration. This is because Silicon has an indirect bandgap at optical communications frequencies and it also does not have a natural electro-optic coefficient. III-V integration on silicon is specially desired due to the increase of interest in shrinking the footprint and improve the energy efficiency of I/Os for the realization of next-generation high performance computing systems.[1,2]

III–V/Si waveguide platforms integration with efficient interconnect access is a technological need due to the emerging of photonic integrated circuits. The silicon-on-insulator (SOI) platform fabrication process is mature by virtue of its compatibility with CMOS technology and because of its small footprint. However, SOI efficient sources are a challenge due to silicon's indirect bandgap. Nevertheless, III-V materials are the industrial standard to produce active devices.[3] One of the main approaches is bonding both III-V and Si chips to produce efficient hybrid devices. They can be directly bonded on silicon (called heterostructure) or butt coupled (called hybrid).[4] Both are subject to misalignment problems - to some extent, and area-on-chip problems. But, even these can be over-sighted by their very large bandwidth.

The heterostructure approach is more likely to be a scalable proposal in terms of overcoming the alignment problem. Recent developments[5] show that alignment problems can also be overcome at the cost of doing the etching process of the III-V layers on top of the silicon-on-insulator platform. Many authors have successfuly demonstrated this kind of processes.[6,7] Nonetheless, they haven't yet optimized their linear transition, resulting

Further author information: (Send correspondence to R.R)
R.R.: E-mail: rrubion@uni.edu.pe, Telephone: +51 988 467 100

Optical Interconnects XXI, edited by Henning Schröder, Ray T. Chen,
Proceedings of SPIE Vol. 11692, 116920T · © 2021 SPIE
CCC code: 0277-786X/21/$21 · doi: 10.1117/12.2577995



(a) III-V to Silicon longitudinal interconnection, 3-D view.

(b) Exploded view of the III-V/Si Transition.

Figure 1: Hybrid interconnection. A total of three tapers were considered: III-V Taper consisting on a spot size converter, a III-V/Si transition with double inverted tapers and Si Taper consisting of Silicon rib waveguide to 450-nm waveguide transition. The linearly varying III-V/Si transition is divided into N segments.

in large structures. When using many sources in dedicated PICs, the miniaturization of these interconnecting structures becomes highly relevant.

Specifically, a very compact vertical interconnecting device was proposed by Huang *et al.*,[8] but the fabrication limit of the III-V mesa was pushed down to 150 nm to obtain an efficient coupling and to keep the silicon core thickness at an standard 220 nm. Interestingly, a 400 nm thick silicon core approach[6] has reportedly better process tolerance than the 220-nm-only devices. The design includes linear adiabatic taper for III-V/Si interfaces, 400 nm-Silicon to 220 nm-Silicon interface, and slim III-V to wide III-V interface. Although wide-band and fabrication tolerant, this approach is not footprint efficient.[9]

We have previously demonstrated[10] a non-linear vertical coupling taper design deterministic methodology, which can ensure an efficient, wide-band, misalignment-tolerant transition between a thin-film polymer on silicon platform to a silicon-on-insulator platform and reduce significantly its footprint. This work, picks up the segmentation methodology, and proposes a compact, ultra wide-band vertical interconnection between a III-V laser platform and a 220 nm-SOI platform based on the Particle Swarm Optimization.

2. III-V TO SOI LONGITUDINAL INTERCONNECTION

The longitudinal interconnection (Fig. 1a) that we optimized consists of three parts: (i) The III-V Taper shrinks the spot size from a 2μm wide III-V active waveguide to a 0.9 μm wide waveguide, the (ii) III-V/Si Transition, couples light from the III-V mesa to a 400-nm-thick silicon rib waveguide. Lastly, (iii) the Si Taper transforms

the rib waveguide to a standard 450-nm-wide SOI channel waveguide. We address the trade-off between coupled power and footprint by using length-optimized tapered segments, as seen in Figure 1b. S_i segments make up the III-V mesa taper, while M_i segments discretize the Silicon rib taper. We propose that each segment should have initial and final fixed widths (white lines), and variable S_i and M_i lengths. Furthermore, note that while the S_i segments initial and final widths decrease, M_i segments initial and final widths increase, progressively. This is because we want to couple light from one platform to the other vertically through their evanescent fields.

According to most III-V laser geometries,[11] a 12 % confinement factor multi-quantum well (MQW) with III-V structured claddings and substrates were used. We also considered a 400 nm-thick silicon rib core with BCB adhesive, the same transition proposed in 7, 11, 12 to relax the lithography requirements for the III-V mesa. Furthermore, the works mentioned above have correctly considered the largest footprint for the III-V/Si transition, above 100 μm long.

Next, we describe our method by optimizing the biggest footprint problem, the III-V/Si transition taper. Subsequently, we will apply our method to optimize the III-V taper and the Si Taper (see Fig. 1a for names and geometric references). Our method is based on the particle swarm optimization of segments S_i and M_i, to maximize transmittance.

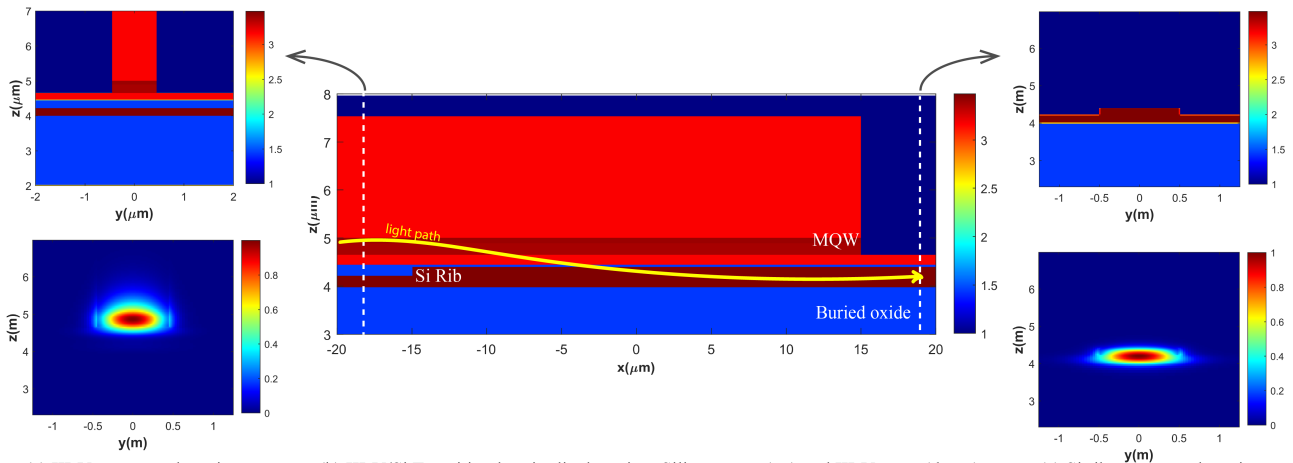
3. PARTICLE SWARM OPTIMIZATION

Particle Swarm Optimization is a technique inspired by the social behavior of bees and has been successfully applied to a wide variety of electromagnetic optimization problems.[13] The swarm population indicates is the number of potential solutions, which are called agents or particles. These particles are initialize at random positions and velocities in the parameter space, then we update the position and velocity according to eq. 1 and eq. 2 respectively as our figure of merti (FOM) converges towards the desired value.

$$x_n = x_n + \Delta t * \nu_n \tag{1}$$

$$\nu_n = \omega\nu_n + c_1 * rand() * (p_{best,n} - x_n) + c_2 * rand() * (g_{best,n} - x_n) \tag{2}$$

where x_n and ν_n are the particle's position and velocity in the n-dimension of the parameter space respectively. This indicates the range where we can find the best solution for each parameter, Δt is the time between measurements, $p_{best,n}$ and $g_{best,n}$ are individual and global best positions, respectively. The first term of eq. 2 is ν_n from previous iteration scaled by ω, which is the inertial weight. c_1 and c_2 quantify the relative "pull" of $p_{best,n}$



(a) III-V transversal section (b) III-V/Si Transition longitudinal section. Silicon taper (up) and III-V taper (down). (c) Si rib transversal section

Figure 2: III-V transition initial and final transversal cuts, and longitudinal refractive index detail.

and $g_{best,n}$, respectively. The two random numbers, $rand()$, are distributed between 0 and 1, which represents the unpredictable behavior of each bee.

We used a PSO implementation that employs default values of ω, c_1 and c_2 that have shown to converge well in many test optimization problems for photonic design applications.[13,14] In our work, thirty individuals were set as population and a maximum of fifty iterations were considered.

4. III-V/SI TRANSITION OPTIMIZATION

The III-V/Si Transition consists of two inverted tapers that couple light vertically from an active section confined mode, as depicted in Figure 2a, to a silicon rib waveguide depicted in Figure 2c. Light can be coupled either from the III-V waveguide to silicon, as depicted by the light path in Figure 2b, or from the silicon platform to the III-V mesa.

In the silicon-on-insulator platform, we considered a buried 2000 nm thick SiO_2, a silicon waveguide slab which is 220 nm thick, with a silicon rib core 400 nm thick. The III-V mesa includes a 200 nm-thick InP slab as cladding (green color in Fig. 1b and transparent in Fig. 1a). All other mesa layers are tapered, including the active layers where the multi-quantum wells are and amplification is carried out. For this experiment, we considered a total active layer thickness of 100 nm. Note that this parameter can change depending on the number of quantum layers and buffer's thickness. Lastly, III-V and Si platforms can be brought together with a BCB; we considered a 50-nm-thick DVS-BCB adhesive.

To define the optimization parameters for the Particle Swarm optimization algorithm, let us divide a linearly-varying III-V/Si Transition into 11 segments and consider each segment length an optimization variable. Note that, we set the total power in the quasi-TE0 mode as FOM.

As a result of the optimization, we propose a non-intuitive III-V/Si transition design. Our new III-V/Si transition is 28.505-μm long. Each segment length is presented in Table 1. Note that corresponding segments S_i and M_i do not necessarily have the same length. It is important to note that both tapers are slowly varying

Table 1: Segment lengths for the optimized 28.505 μm long III-V/Si transition.

Segment length [μm]	S_1 1.5	S_2 3.5	S_3 3.5	S_4 3.5	S_5 3.5	S_6 2.715	S_7 1.5	S_8 1.5	S_9 3.5	S_{10} 1.5	S_{11} 1.5
Segment length [μm]	M_1 1.5	M_2 1.5	M_3 1.5	M_4 3.5	M_5 3.5	M_6 3.5	M_7 3.5	M_8 3.5	M_9 3.5	M_{10} 1.5	M_{11} 1.505

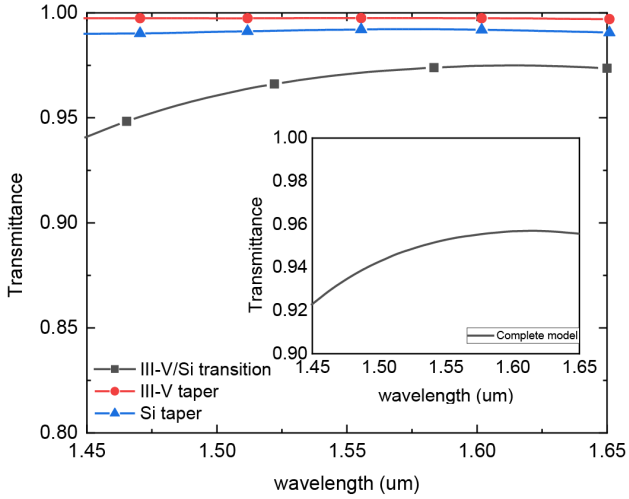
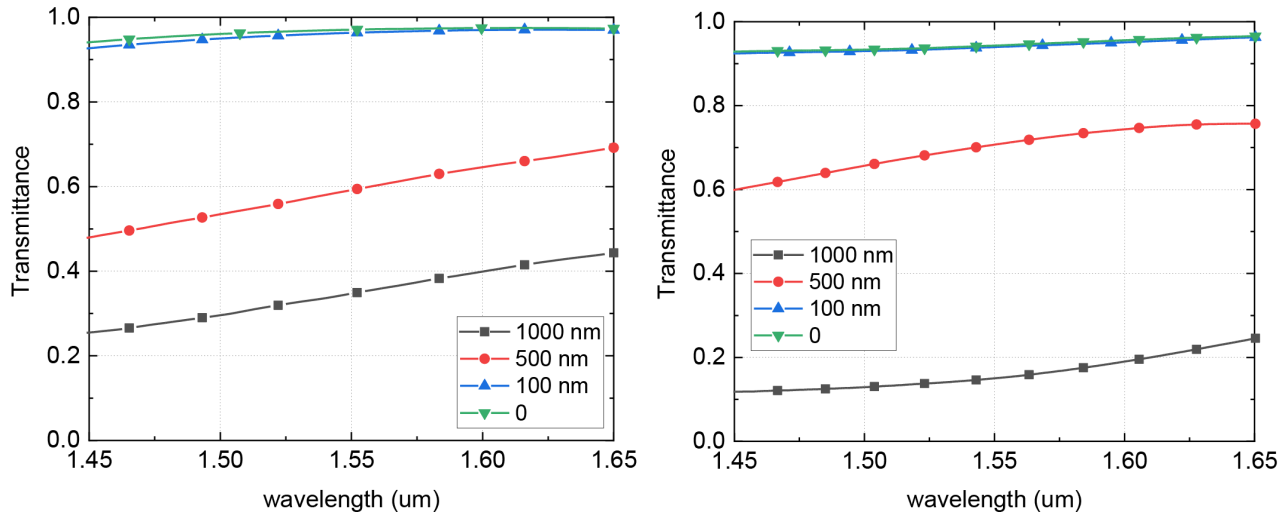


Figure 3: Transmittance of our optimized tapers. Si taper is the rib to channel silicon converter, III-V/Si transition is where light is coupled vertically between the two platforms, and III-V taper is a spot size converter within the active region.



(a) Our model. 28.505 μm long

(b) 100μm-long taper.

Figure 4: Waveband analysis as function of horizontal misalignment up to 1000 nm. "0" indicates the ideal case, where there is zero horizontal misalignment.

in slightly wider regions while varying faster towards their corresponding slimmer regions. This is evident in segments S_2, S_3, S_4, S_5 and segments M_5, M_6, M_7, M_8, M_9 in III-V and silicon tapers, respectively.

According to Figure 3, III-V/Si transition transmittance is above 94% for the S, C and L fiber optic communications band. Furthermore, the other two tapers (lines with circles and triangles, respectively) were also optimized using the same technique, producing 17.45 μm and 19.37 μm long Silicon taper and III-V taper, respectively. Thus, we coupled light from a III-V active mesa to a traditional silicon-on-insulator channel waveguide in 65.325 μm. With the aforementioned complete model, we achieved 94.4% transmittance at 1550 nm.

Although, for linear tapers, there is usually a clear trade-off between adiabatic transition and transmitted power, we demonstrate that this non-intuitive geometry is more than three times smaller than the state of the art for adiabatic III-V/Si evanescent couplers.[7,11] A direct comparison to a linear model is presented in Figure 4. We can see similar waveband behavior of our model to a 100 μm long linearly varying III-V/Si transition taper, even with more than three times smaller footprint. 3D FDTD simulations were carried out for this analysis.

5. FEASIBILITY

The minimum dimensions of our proposed model are compatible with deep-UV lithography. Silicon-on-insulator geometries can be defined previous to the III-V die bonding.[4,11] The bonding process is feasible following the die-to-wafer bonding process by using an adhesive with a matching SOI cladding refractive index. The III-V epitaxial layer geometry can be lithographed on top, after the bonding process is done.

Depending on the adhesive deposition technique, some hybrid devices work with less than the 50 nm-thick adhesive described here, such as 35-nm DVS-BCB,[15] and 25-nm spray-coated BCB.[16] Slimmer adhesives can improve the results of our methodology and shrink the dimensions of the III-V/Si transition further.

6. MISALIGNMENT STUDY

Fabrication approaches like heterogeneous bonding or epitaxial growth[17,18] have a high alignment accuracy, down to tens of nanometers. However, other techniques compatible with CMOS processes, like flip-chip bonding[19] are not that precise, and they have potential horizontal misalignments that go up to micron size. Although epitaxial growth is the technology that offers the highest integration, it has been mostly demonstrated inside the lab, while flip-chip techniques are well-established in the industry. Both approaches can be used with reliability.

We present the effects of fine and coarse III-V and Silicon platforms horizontal misalignments applied to our proposed models and compare their tolerance to traditional linearly varying approaches.

Our model, as depicted in Figure 4a, has a high tolerance for small misalignments up to 100 nm, with a calculated power compromise smaller than 1%. A more pronounced flip-chip related misalignment, progressively compromises up to approximately 50% of the total power. Compared to a 100 μm-long linear taper (Fig. 4b), we believe that there is a sweet spot for footprint/misalignment trade-off, specially towards the range from 500 to 1000 nm of horizontal misalignment. As stated in the feasibility section, these calculations can still improve, by using our proposed methodology with thinner adhesives, depending on the fabrication capabilities.

7. CONCLUSION

We propose an optimization model to produce non-intuitive III-V-to-SOI transition using the Particle Swarm Optimization. Our applied results show a three times smaller non-linearly varying taper that maintains a planar transmittance response beyond the S, C and L optical communications bands above 94%. Furthermore, our methodology is feasible, compatible with UV-lithography and other CMOS processes. In the field of heterogeneous integration, our methodology can be compared with a 100 μm-long linear taper in terms of robustness against misalignment for different bonding technologies. We demonstrated our model's superior robustness for above-500-nm horizontal misalignment cases.

ACKNOWLEDGMENTS

The authors would like to acknowledge the funding from the British Council, Newton Mobility Grants 2018 Round 1, number NMG \ R1 \ 180035. This work was supported by the Brazilian Agency CNPq under Projects No 465757/2014-6 (INCT FOTONICOM) and No 312714/2019-2 (HEHF's Research Productivity Grant); and by the Sao Paulo Research Foundation (FAPESP) under Project No 2015/24517-8 (Thematic Project "Photonics for Next Generation Internet").

REFERENCES

[1] Bergman, K., Conte, T., Gara, A., Gokhale, M., Heroux, M., Kogge, P., Lucas, B., Matsuoka, S., Sarkar, V., and Temam, O., "Future high performance computing capabilities: Summary report of the advanced scientific computing advisory committee (ascac) subcommittee," tech. rep., USDOE Office of Science (SC)(United States) (2019).

[2] Bergman, K., Shalf, J., and Hausken, T., "Optical interconnects and extreme computing," *Optics and Photonics News* **27**(4), 32–39 (2016).

[3] Agrell, E., Karlsson, M., et al., "Roadmap of optical communications," *Journal of Optics* **18**(6), 063002 (2016).

[4] Roelkens, G., Liu, L., Liang, D., Jones, R., Fang, A., Koch, B., and Bowers, J., "Iii-v/silicon photonics for on-chip and intra-chip optical interconnects," *Laser & Photonics Reviews* **4**(6), 751–779 (2010).

[5] Ng, D. K. T. et al., "Demonstration of heterogeneous iii-v/si integration with a compact optical vertical interconnect access," *Opt. Lett.* **38**, 5353–5356 (Dec 2013).

[6] Roelkens, G. et al., "Iii-v-on-silicon photonic integrated circuits for optical interconnects," in [*Summer Topicals Meeting Series (SUM), 2015*], 144–145, IEEE (2015).

[7] De Rezende, G. F., Frateschi, N. C., and Roelkens, G., "Tunable iii-v-on-si laser with resonant photonic molecule mirrors," in [*CLEO: Science and Innovations*], STu3N–2, Optical Society of America (2019).

[8] Huang, Q. et al., "Ultracompact tapered coupler for the si/iii–v heterogeneous integration," *Applied optics* **54**(14), 4327–4332 (2015).

[9] Wang, Q. et al., "Heterogeneous si/iii-v integration and the optical vertical interconnect access," *Optics Express* **20**(15), 16745–16756 (2012).

[10] Rubio-Noriega, R. E. and Hernández-Figueroa, H. E., "Compact low loss vertical coupling for optical transmitters with polymer modulators," *J. Lightwave Technol.* **35**, 5440–5447 (Dec 2017).

[11] Roelkens, G., Abassi, A., Cardile, P., Dave, U., De Groote, A., De Koninck, Y., Dhoore, S., Fu, X., Gassenq, A., Hattasan, N., et al., "Iii-v-on-silicon photonic devices for optical communication and sensing," in [*Photonics*], **2**(3), 969–1004, Multidisciplinary Digital Publishing Institute (2015).

[12] Wang, Z., Abbasi, A., Dave, U., De Groote, A., Kumari, S., Kunert, B., Merckling, C., Pantouvaki, M., Shi, Y., Tian, B., et al., "Novel light source integration approaches for silicon photonics," *Laser & Photonics Reviews* **11**(4), 1700063 (2017).

[13] Robinson, J. and Rahmat-Samii, Y., "Particle swarm optimization in electromagnetics," *IEEE transactions on antennas and propagation* **52**(2), 397–407 (2004).

[14] Parsopoulos, K. E., [*Particle swarm optimization and intelligence: advances and applications: advances and applications*], IGI global (2010).

[15] Keyvaninia, S., Verstuyft, S., Van Landschoot, L., Lelarge, F., Duan, G.-H., Messaoudene, S., Fedeli, J., De Vries, T., Smalbrugge, B., Geluk, E., et al., "Heterogeneously integrated iii-v/silicon distributed feedback lasers," *Optics letters* **38**(24), 5434–5437 (2013).

[16] Rimböck, J., Gasiorowski, J., Pires, M., Zenger, T., Burggraf, J., and Dragoi, V., "Adhesive wafer bonding using ultra-thin spray-coated bcb layers," *ECS Transactions* **98**(4), 67 (2020).

[17] Feifel, M., Ohlmann, J., Benick, J., Hermle, M., Belz, J., Beyer, A., Volz, K., Hannappel, T., Bett, A. W., Lackner, D., et al., "Direct growth of iii–v/silicon triple-junction solar cells with 19.7% efficiency," *IEEE Journal of Photovoltaics* **8**(6), 1590–1595 (2018).

[18] Ramirez, J. M., Elfaiki, H., Verolet, T., Besancon, C., Gallet, A., Néel, D., Hassan, K., Olivier, S., Jany, C., Malhouitre, S., et al., "Iii-v-on-silicon integration: From hybrid devices to heterogeneous photonic integrated circuits," *IEEE Journal of Selected Topics in Quantum Electronics* **26**(2), 1–13 (2019).

[19] Roelkens, G., Van Campenhout, J., Brouckaert, J., Van Thourhout, D., Baets, R., Romeo, P. R., Regreny, P., Kazmierczak, A., Seassal, C., Letartre, X., et al., "Iii-v/si photonics by die-to-wafer bonding," *Materials Today* **10**(7-8), 36–43 (2007).